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52	PWR_12V OCP - UP6273A
53	CPU_PWR_VCCIO - NB681G
54	CPU_PWR_ST/PLL
55	CPU_PWR_SA-RT8125E
56	DDR4 Power-RT8125E
57	DDR4 Power-VEP25
58	PCH Core Power-RT8125E
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65	Power Sequence
66	Revision History

MS-7B61

Ver: 1.0 ATX
PCB size : 304.8mm * 243.84mm

Intel - Kaby Lake Z370

CPU:

Coffee Lake S

System Chipset:

Z370

Onboard Chip:

HD Audio Codec : ALC892

LAN : intel I219V

SIO : Nuvoton 6795

Flash ROM : 16MB Z270

Main Memory:

*DDRIV (800/1066/1333/1600/2133/2400MHz) * 4 (Dual Channel)*

ACPI:

NIKO/UPI

PWM:

UPI9508

Expansion Slots:

*PCI Express (X16) Slot *1*

*PCI Express (X4) Slot *1*

*PCI Express (X1) Slot *4*

*M2 M-Key *1*

Other:

*SATA3.0 *6*

*FRONT USB2.0 *4*

*FRONT USB3.0 *4*

*REAR USB3.0 GEN1 Z270 *4*

*REAR USB2.0 *2*

Display :

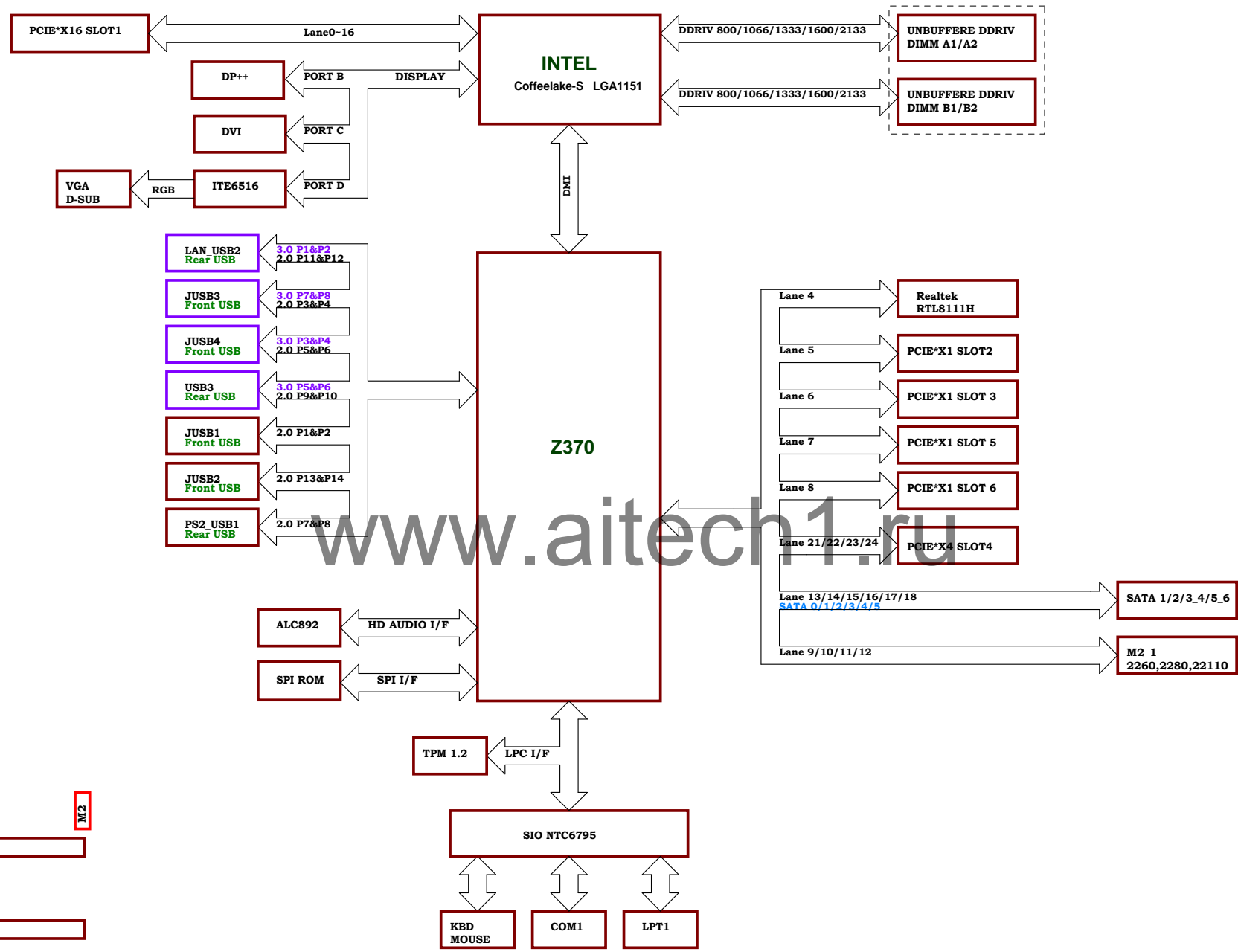
DISPLAY PORT

DVI

VGA-ITE6516 DDI to D-SUB

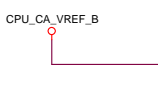
MICRO-STAR INT'L CO.,LTD		
MS-7B61		
Size Custom	Document Description Cover Sheet	Rev 1.0
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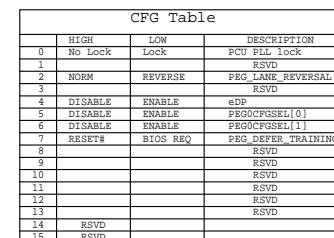
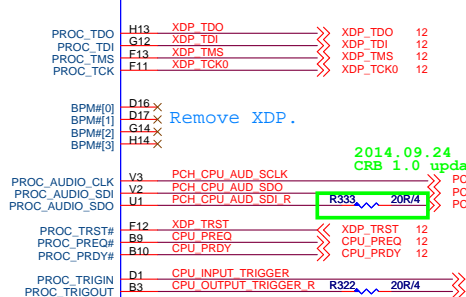
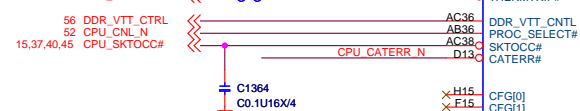
MS-7B61 Block Diagram



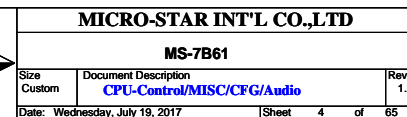
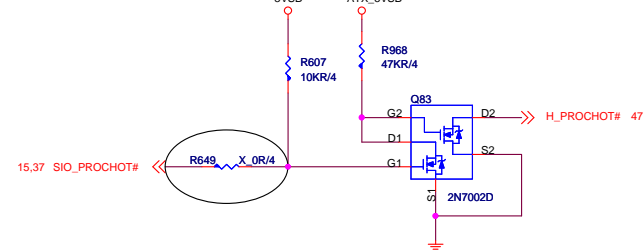
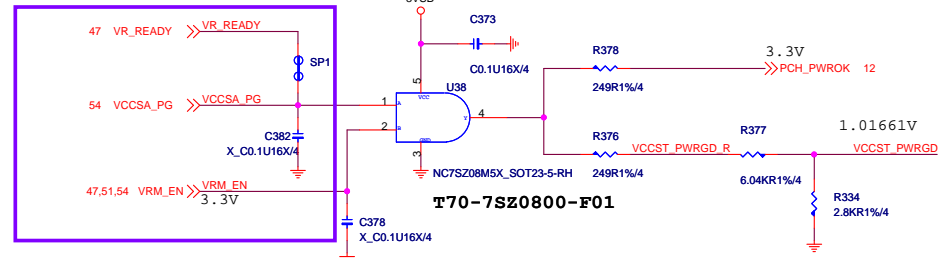
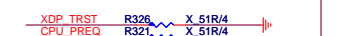
Slot Sequence:

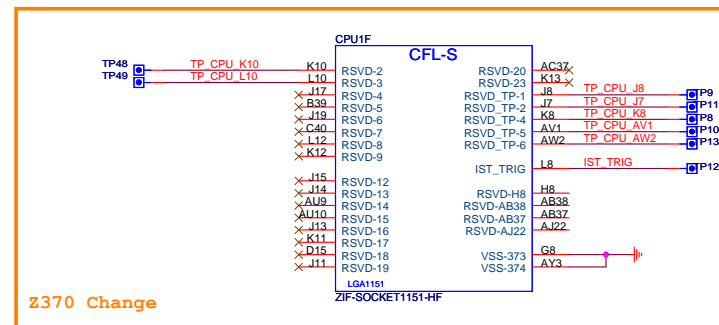
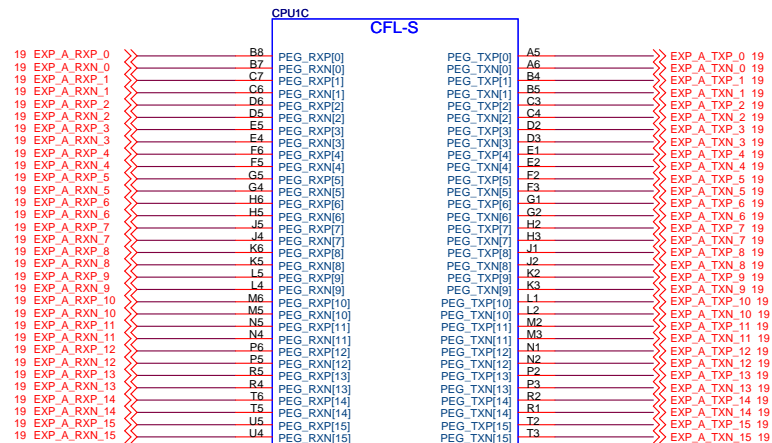
M2_1	22110	M2
PCie_E1	CPU PCie X16	
PCie_E2	PCie X1	
PCie_E3	PCie X1	
PCie_E4	PCie X4	
PCie_E5	PCie X1	
PCie_E6	PCie X1	





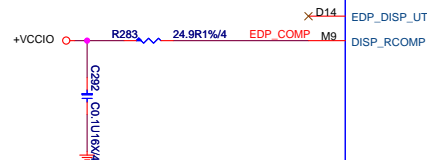
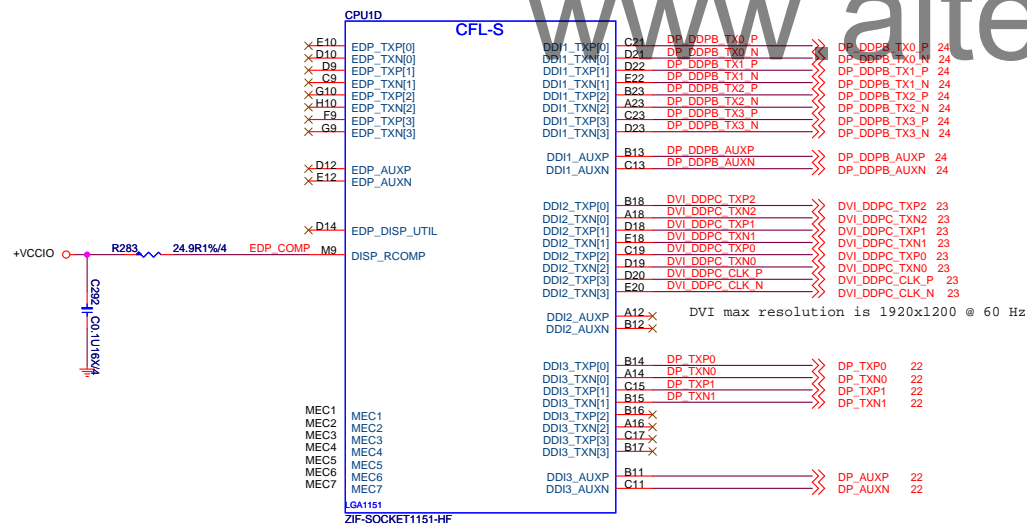
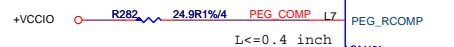
1000 mil < CPU_XDP_MBP0~1 < 6000 mil





Z370 Change

TP8, TP9, TP10, TP11, TP12, TP13, TP48, TP49
Reservd for CPU XDP debug pin



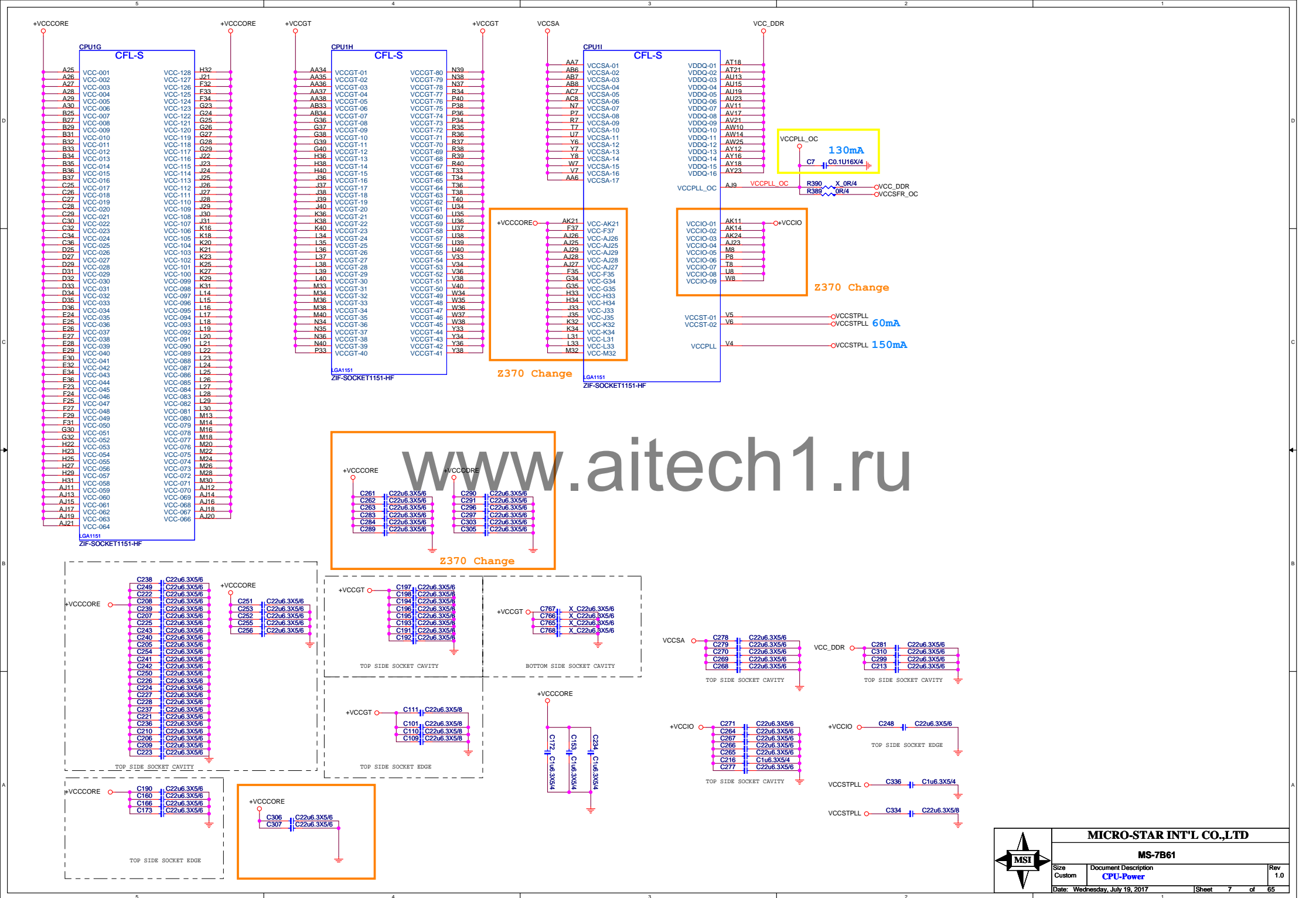
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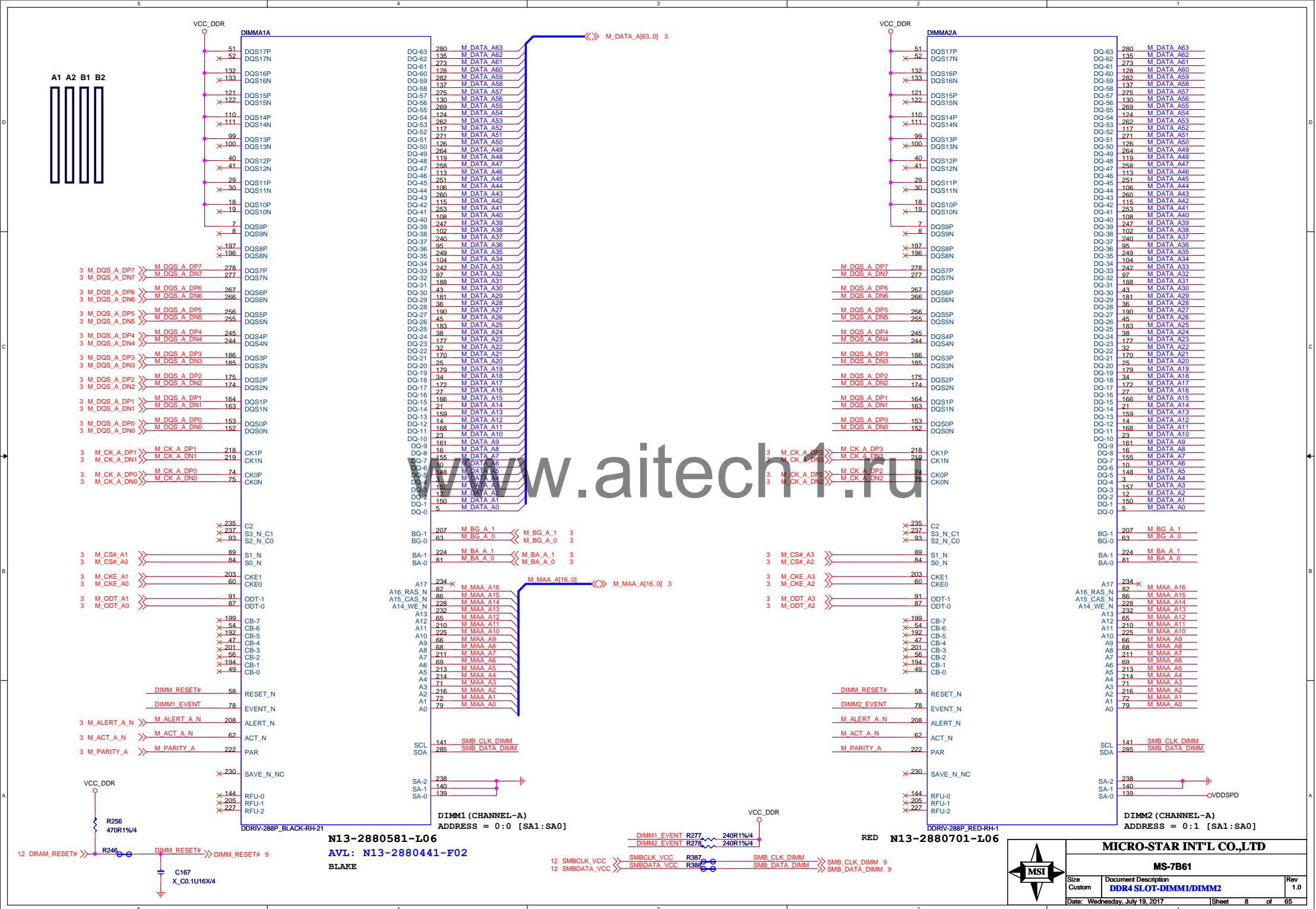


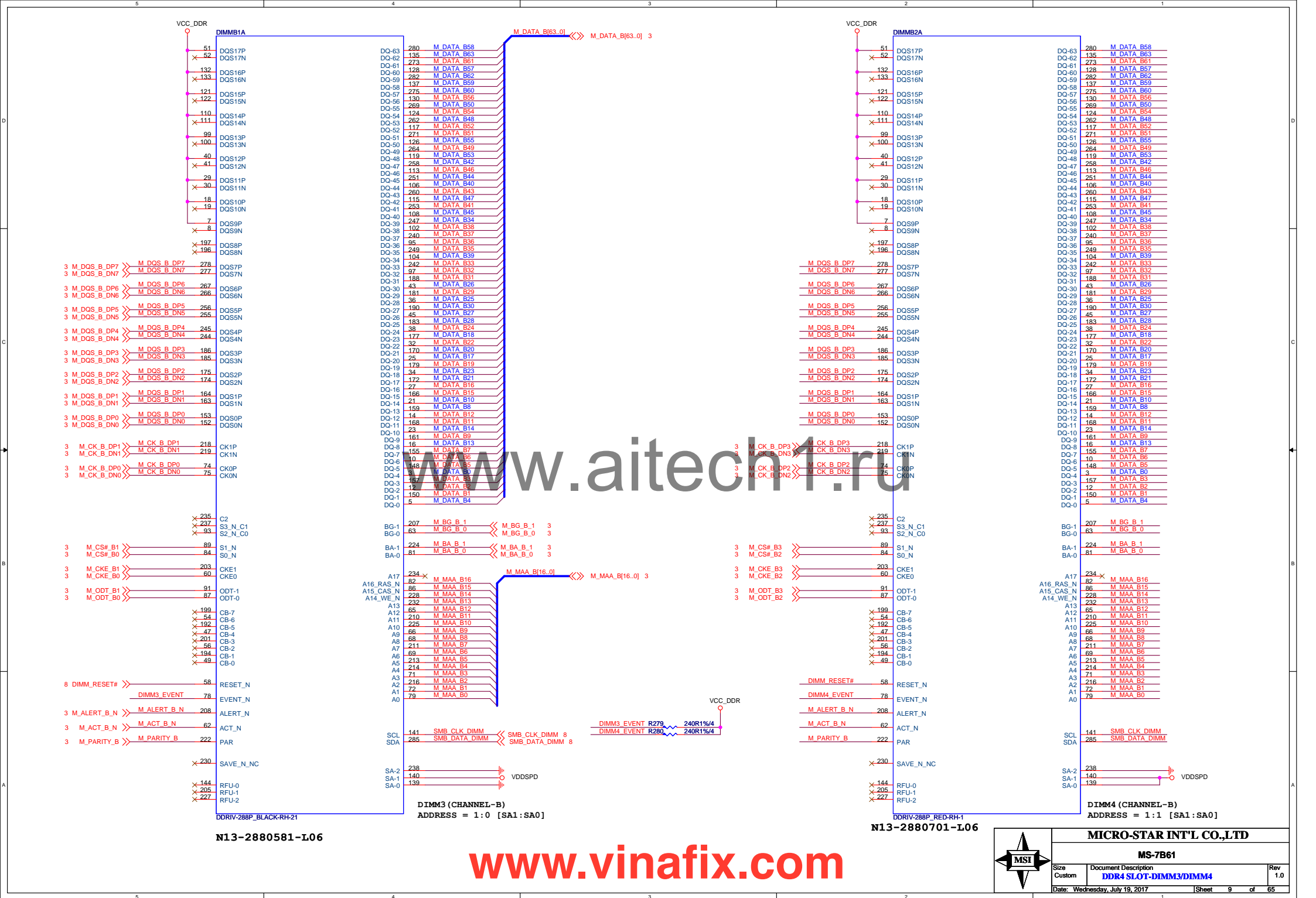
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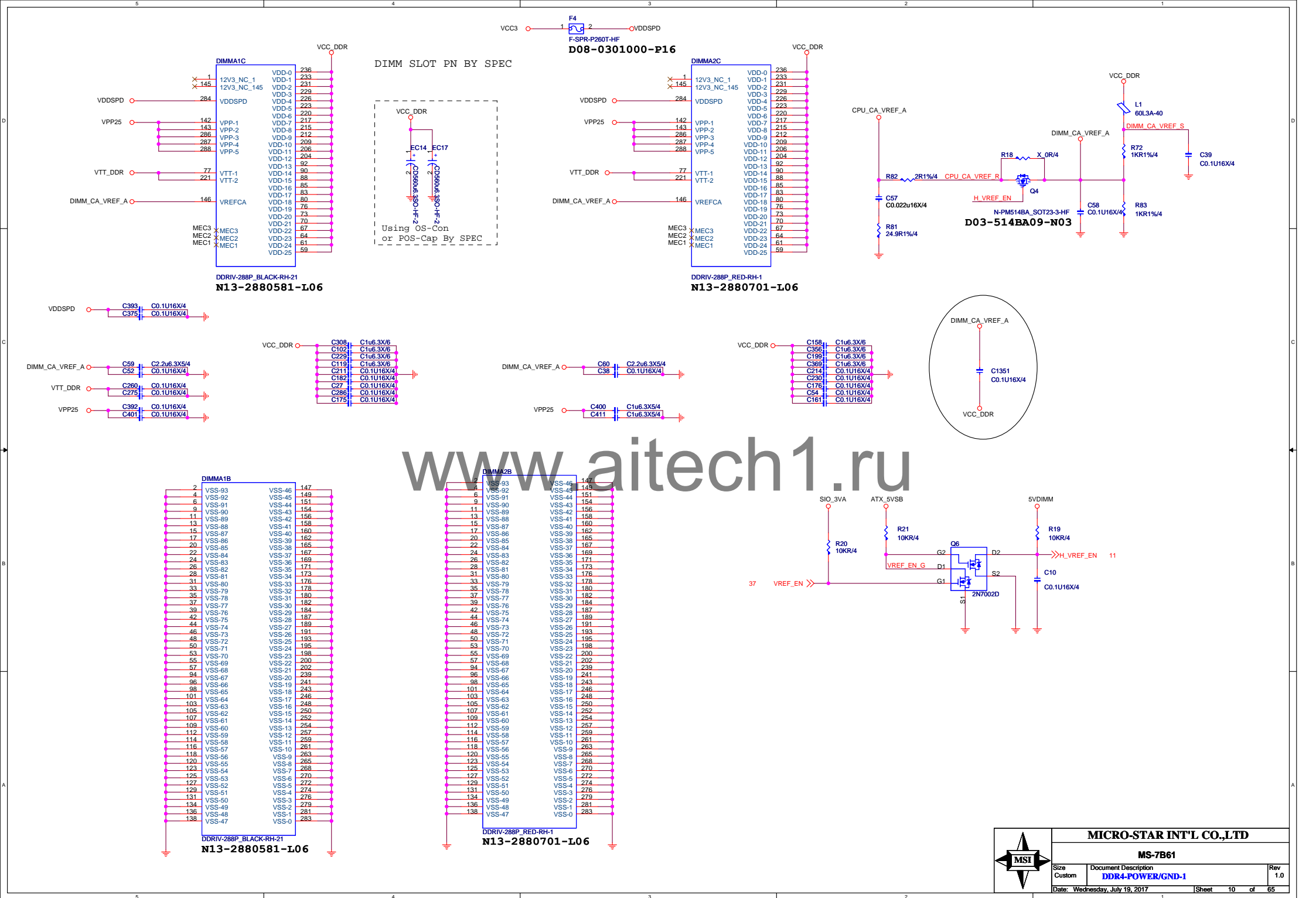
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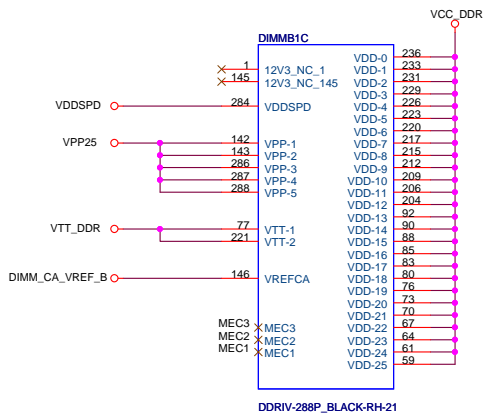
N13-2880701-L06

www.vinafix.com

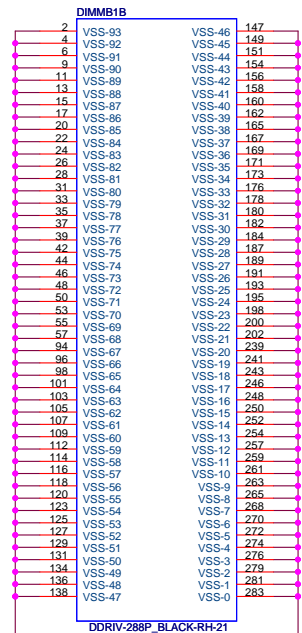
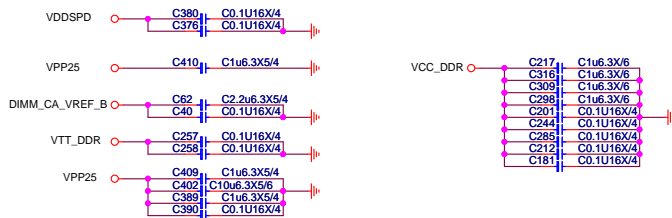


MICRO-STAR INT'L CO.,LTD		
MS-7B61		
Size	Document Description	Rev
Custom	DDR4 SLOT-DIMM3/DIMM4	1.0
Date: Wednesday, July 19, 2017		Sheet 9 of 65

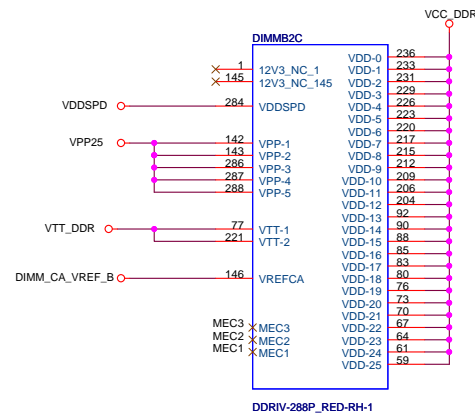




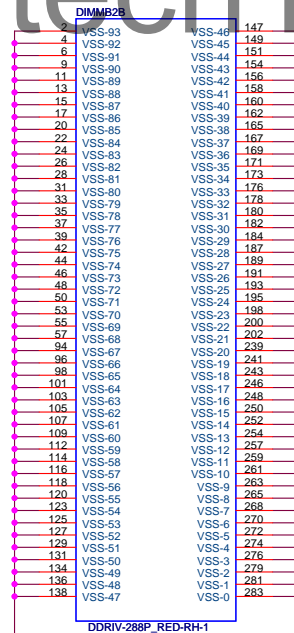
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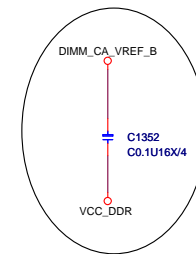
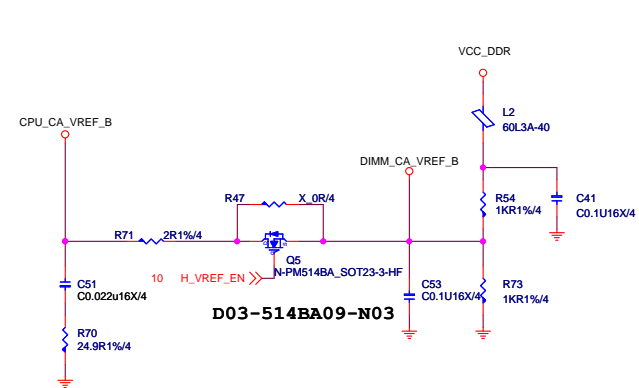
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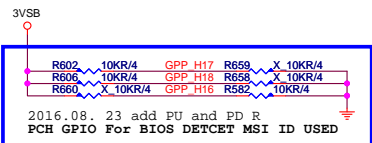
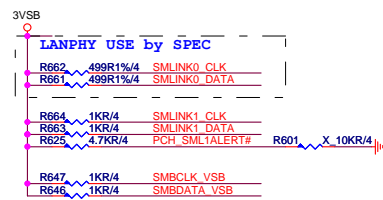
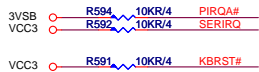
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N13-2880701-L06

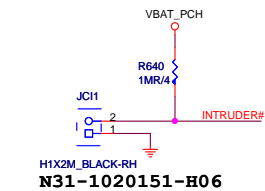


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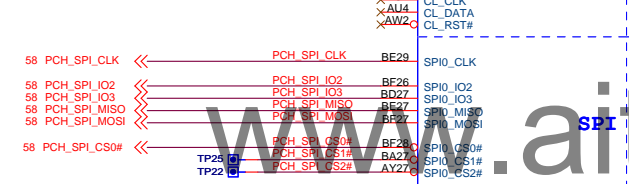
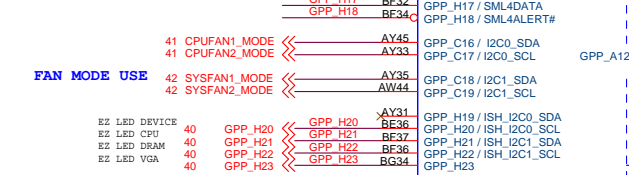
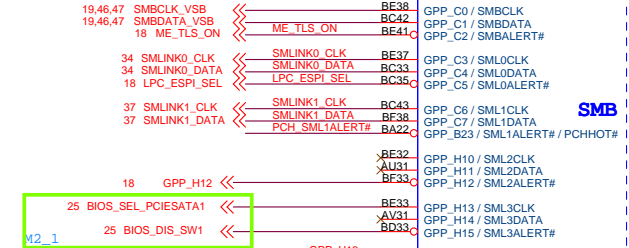
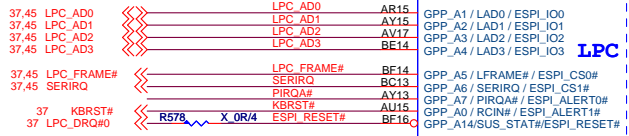
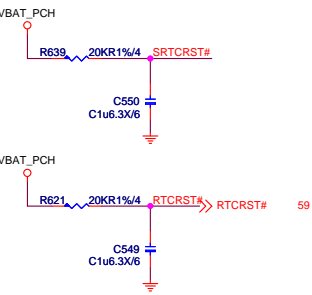


GPP_H18
HIGH : NA ASM2142
LOW : BIOS running ASM2142 A0,A1 path code

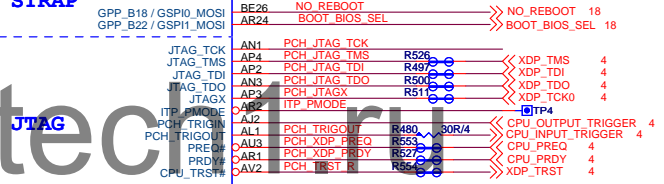
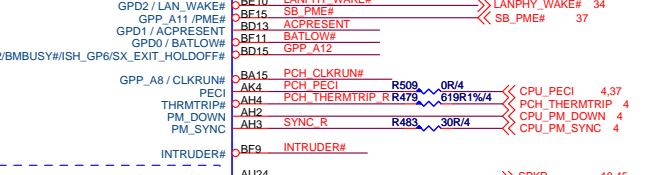
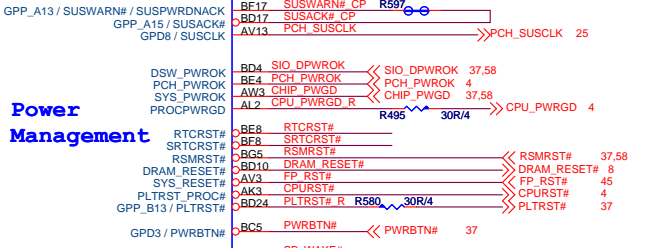
Chassis Intrusion



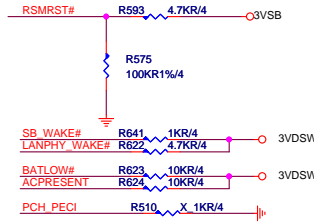
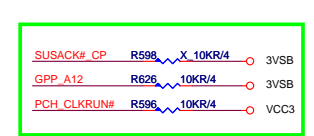
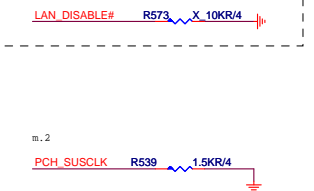
RTC



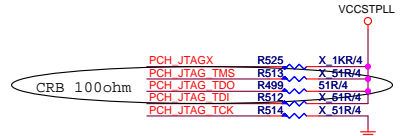
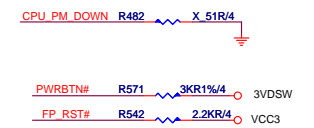
B01-2Z37005-I06



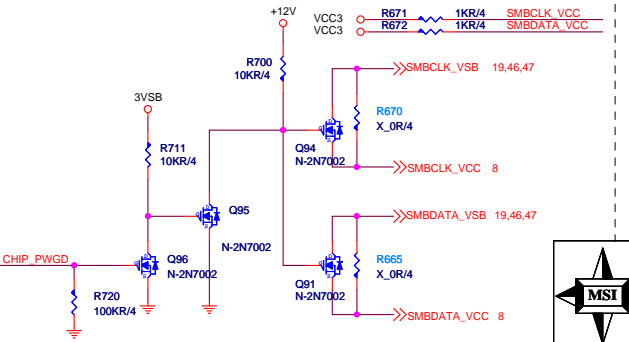
PCH_LANPHY_PWR
Pull Down PCH PHY into low power state.
For No Use Intel Lan



SB_PME#
Internal Pull high
100 series PCB no boot issue
used external pull-high



擺在一起 (注意到所有的SMBUS的分枝)

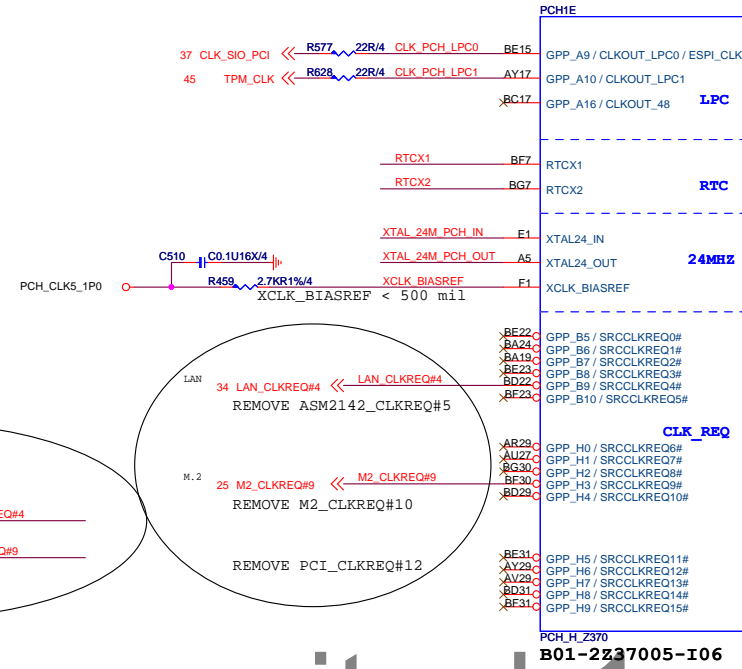
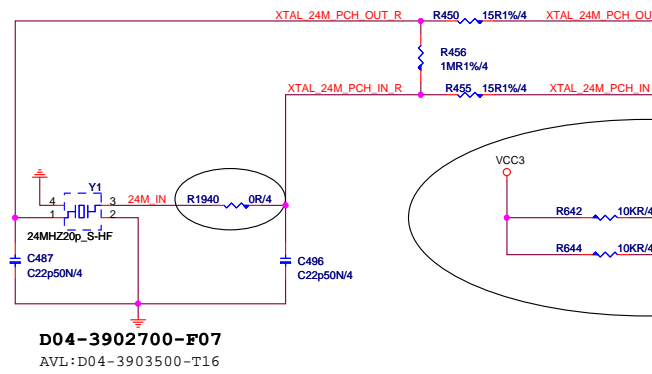
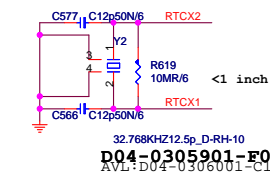


MICRO-STAR INT'L CO.,LTD		
MS-7B61		
Size	Document Description	Rev
Custom	PCH-LPC/SPI/SMBUS/MISC	1.0
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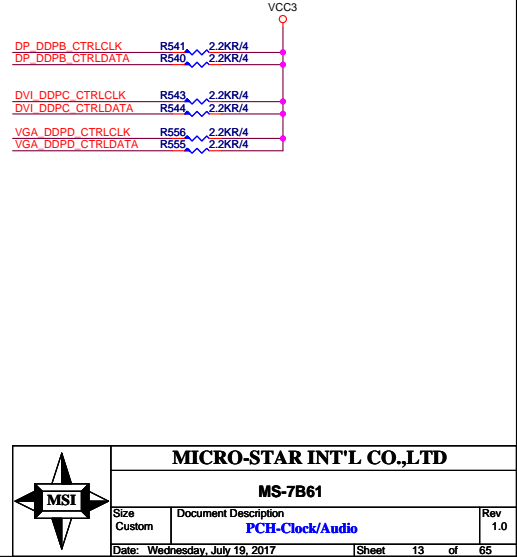
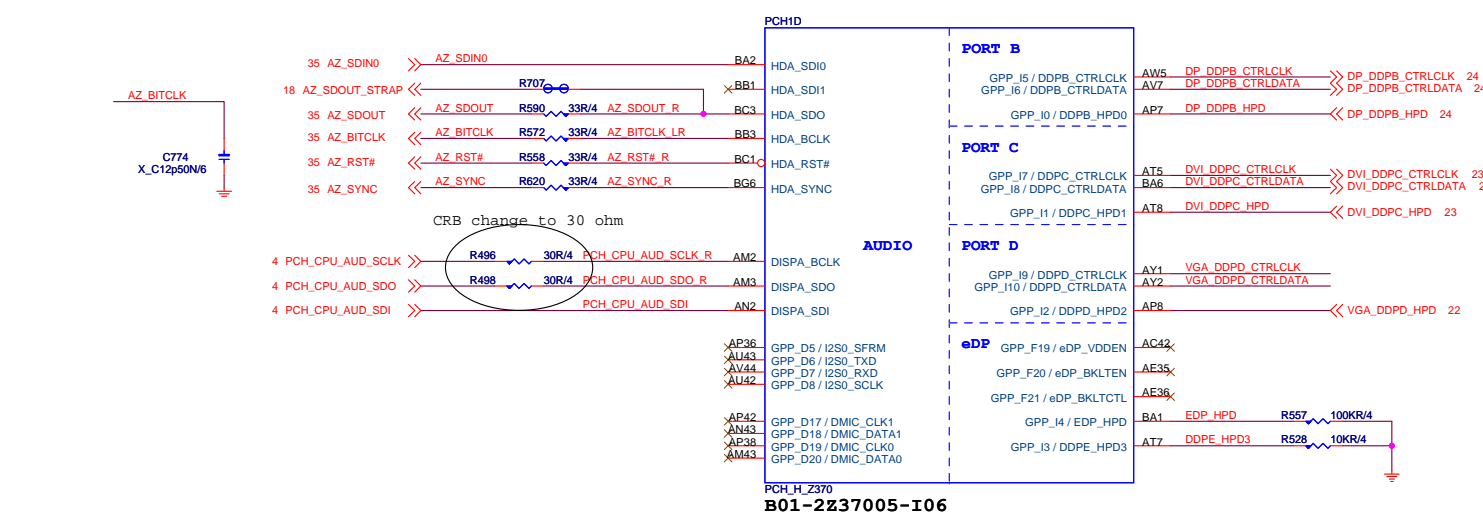
PCH_CLK

RTC Block

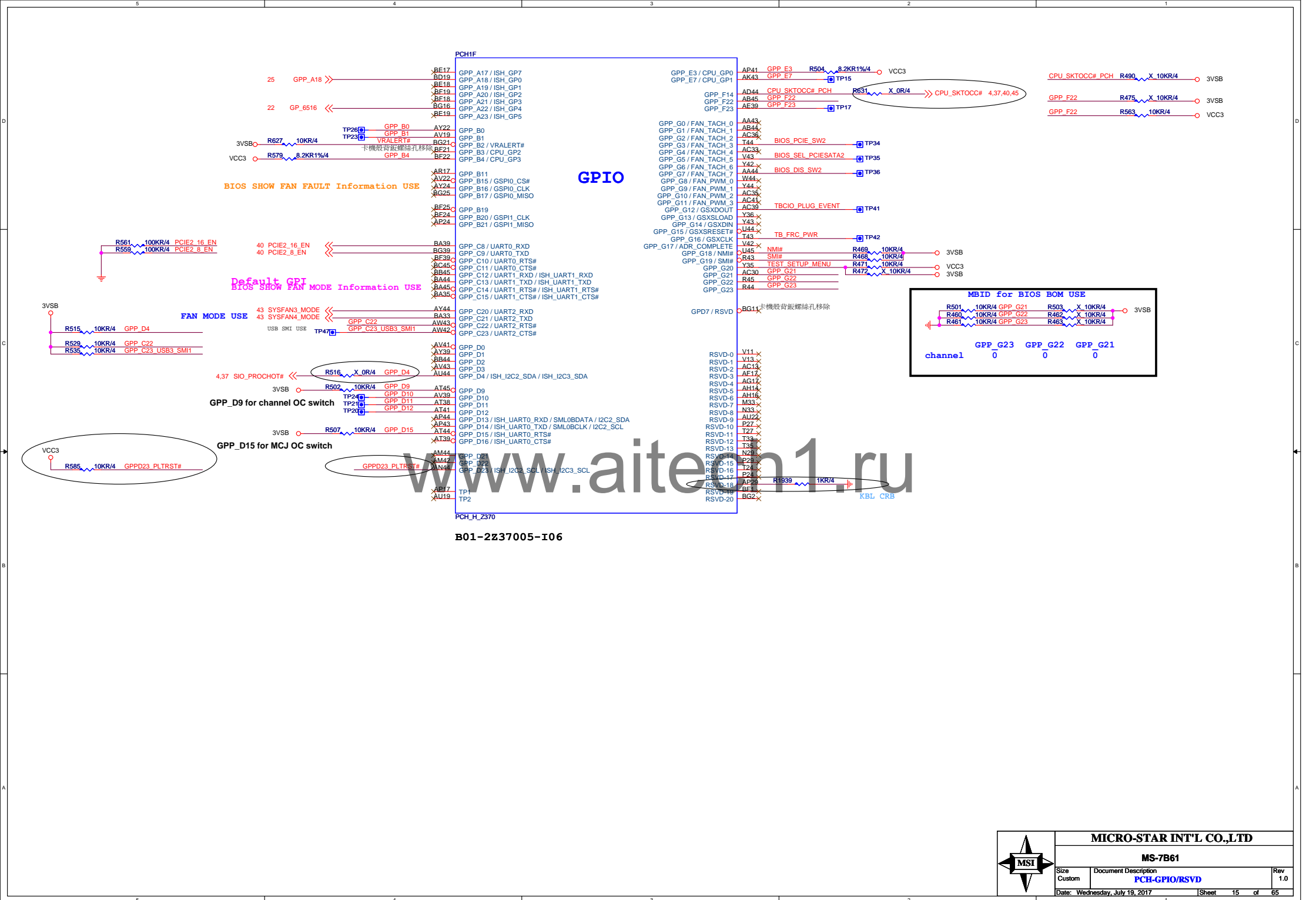
Close to PCH

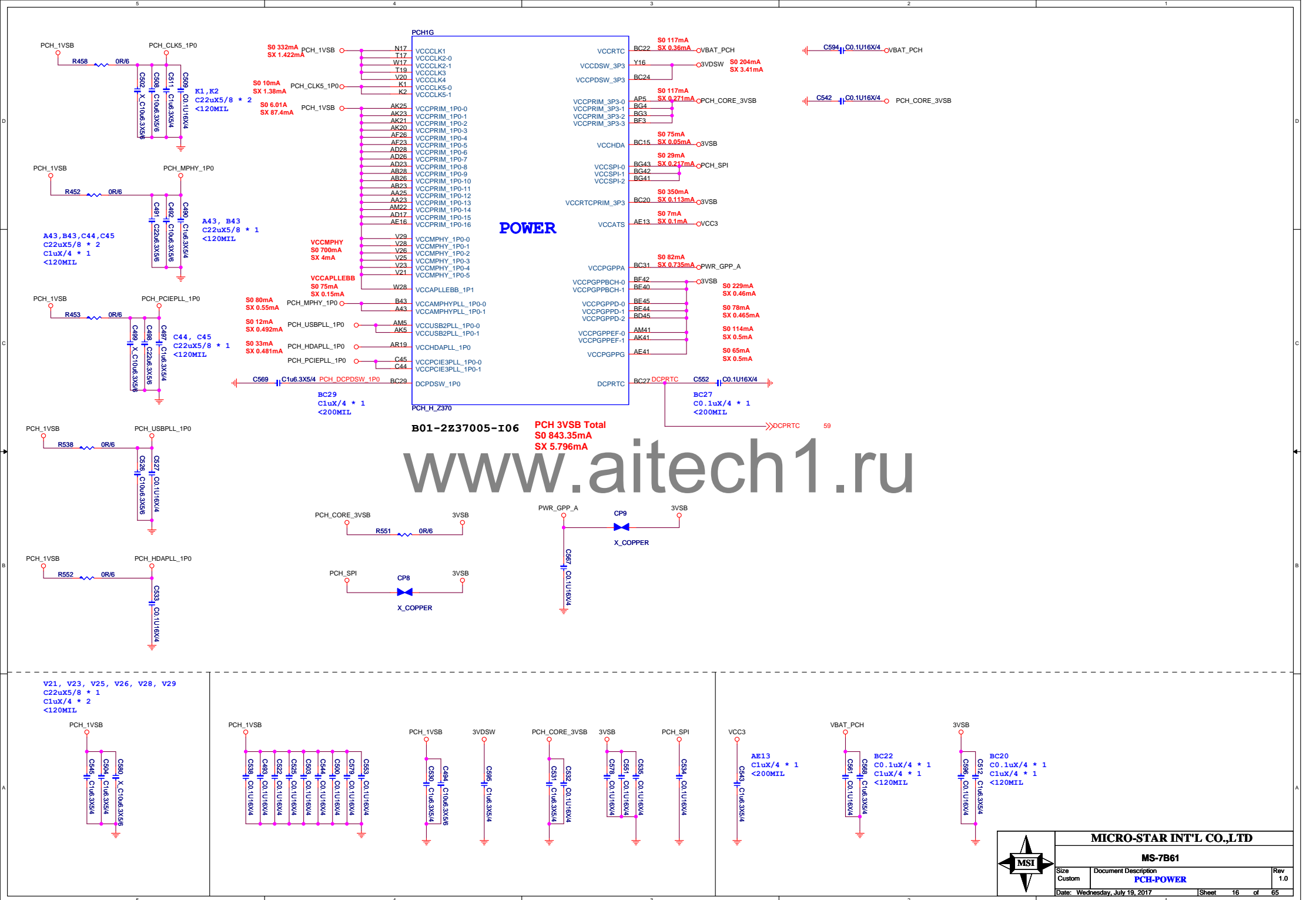


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MS-7B61		
Size	Document Description	Rev
Custom	PCH-Clock/Audio	1.0
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MICRO-STAR INT'L CO.,LTD

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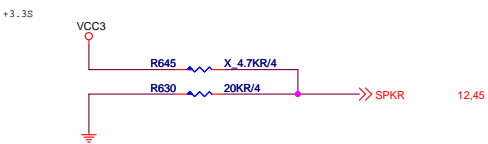
Size Custom	Document Description PCH-POWER	Rev 1.0
Date: Wednesday, July 19, 2017		Sheet 16 of 65



B01-2Z37005-I06

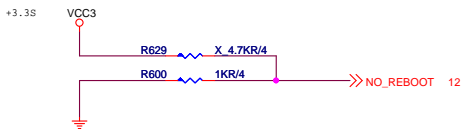
	MICRO-STAR INT'L CO.,LTD			
	MS-7B61			
	Size	Document Description	Rev	
	Custom	PCH-GND	1.0	
	Date: Wednesday, July 19, 2017		Sheet	17 of 65

TOP Swap



Internal pull-down is disabled after PLTRST#

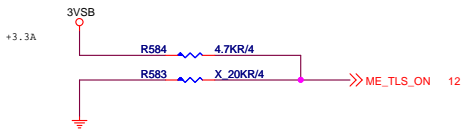
No Reboot



```
0 : DISABLE (Default)
1 : ENABLE
```

Internal pull-down is disabled after PLTRST#

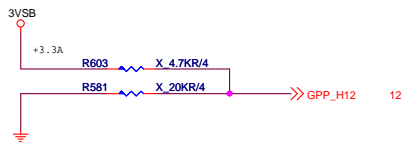
AMT and SBA with confidentiality



```
0 : DISABLE
1 : ENABLE (Default)
```

Internal pull-down is disabled after RSMRST

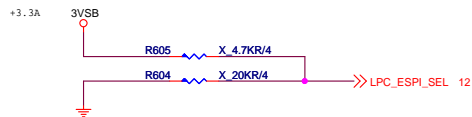
ESPI FLASH SHARING MODE



```
0 : MASTER ATTACHED FLASH SHARING
1 : SLAVE ATTACHED FLASH SHARING
```

Internal pull-down is disabled after RSMRST

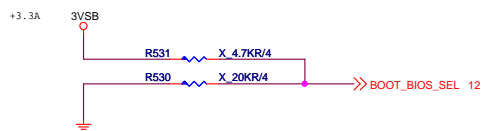
LPC eSPI Mode



```
0 : LPC
1 : eSPI
```

Internal pull-down is disabled after RSMRST

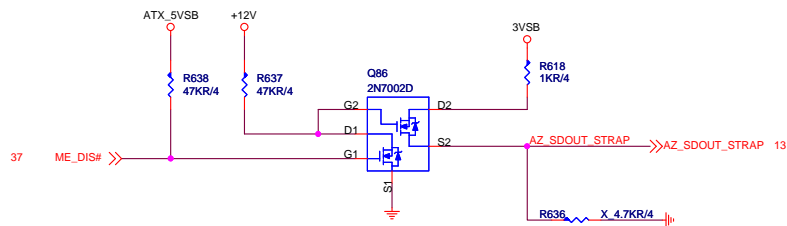
Boot BIOS



```
0 : SPI
1 : LPC
```

Internal pull-down is disabled after PLTRST

HDA_SDO

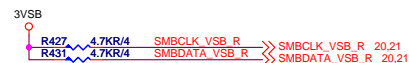


MICRO-STAR INT'L CO.,LTD

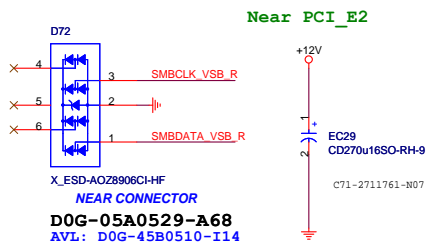
MS-7B61

Size Custom	Document Description PCH-Strap	Rev 1.0
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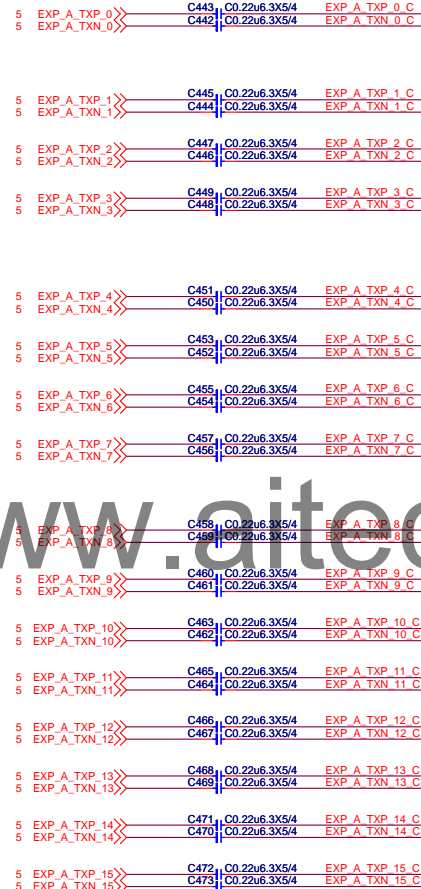
12V - 5.5A
VCC3 - 3A
3VSB - 375mA



2016.06.23
Compatibility issue of 10G LAN Card and Gigabyte VGA Card
0R and TVS reserved and not on the part

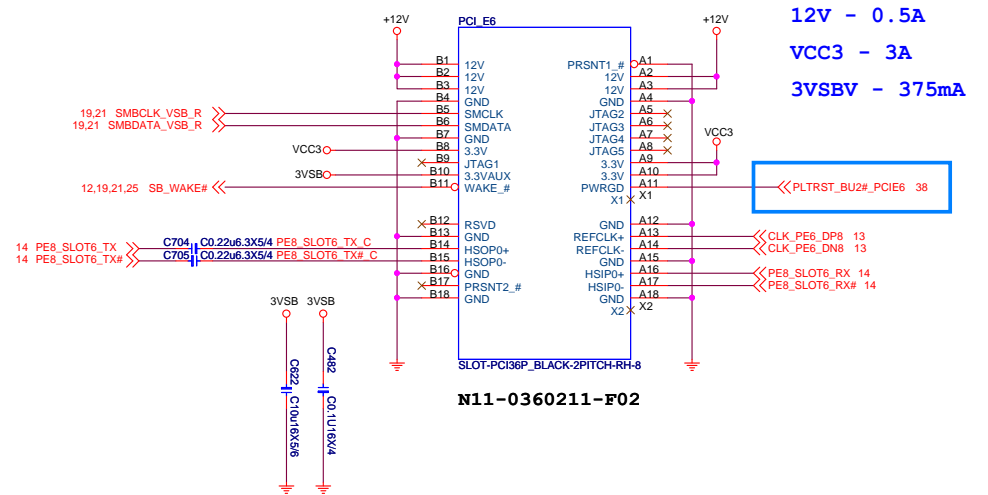
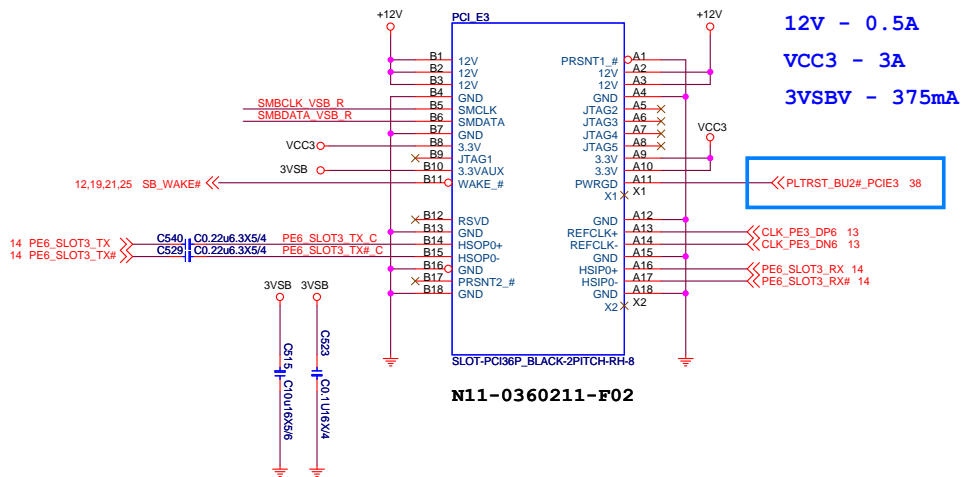
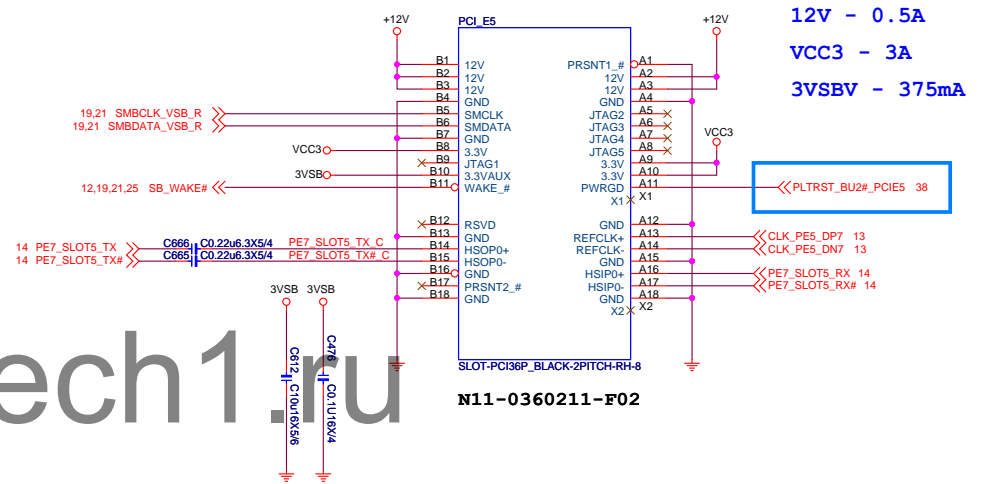
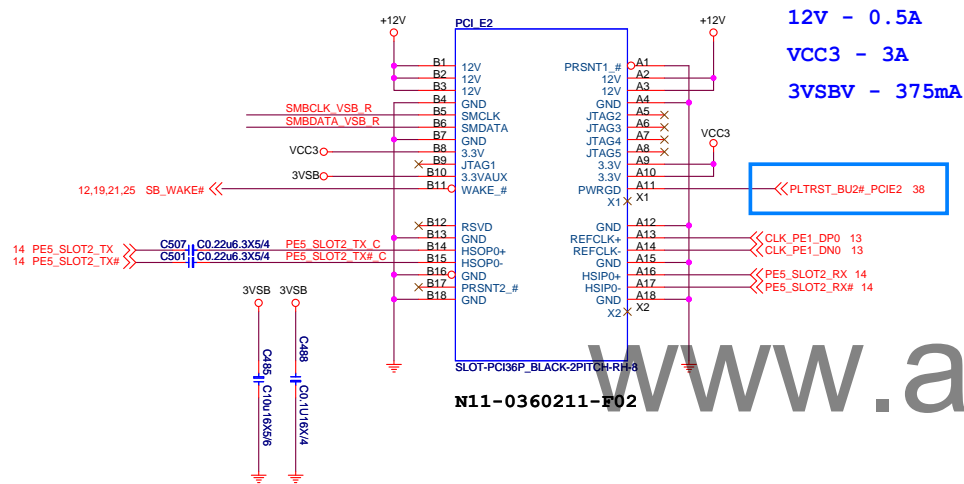


12,20,21,25 SB_WAKE# <<

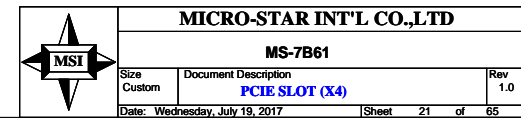


N11-1641671-L06

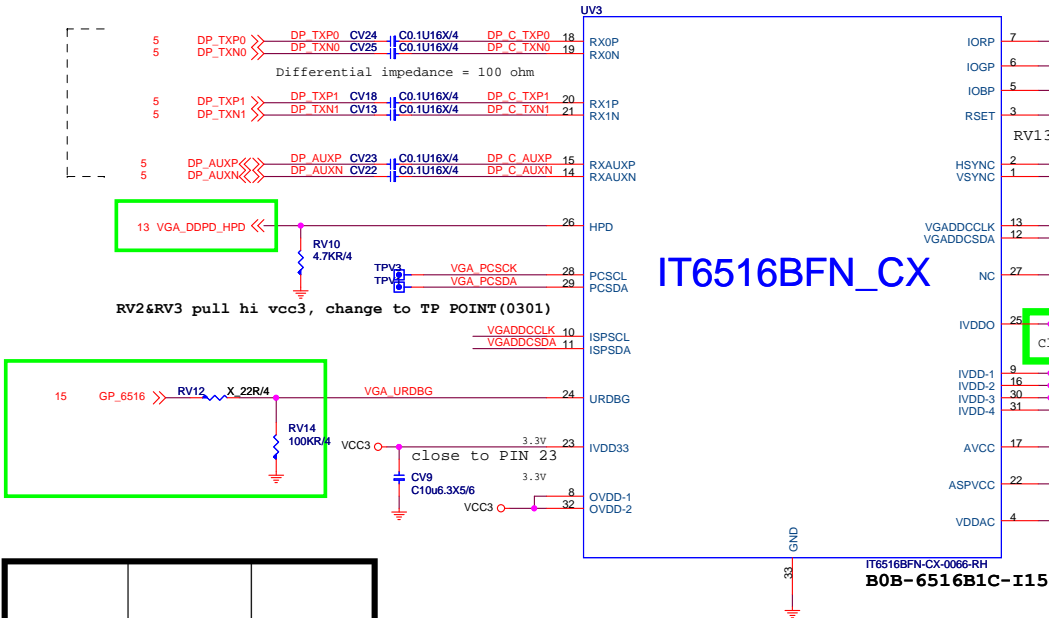
MICRO-STAR INT'L CO.,LTD			
MS-7B61			
Size	Document Description	Rev	
Custom	PCIE SLOT (X16)	1.0	
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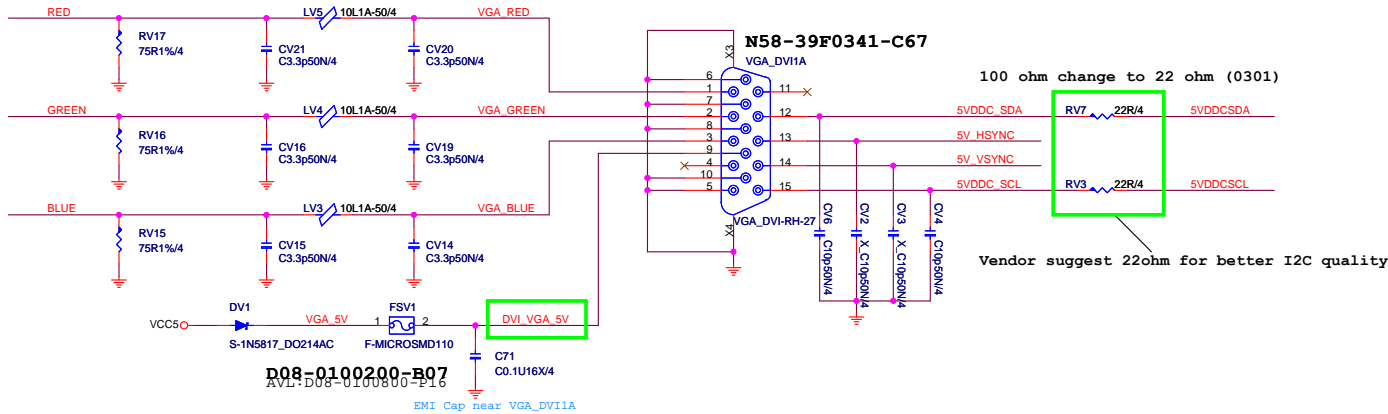
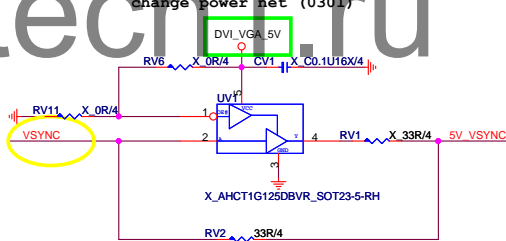
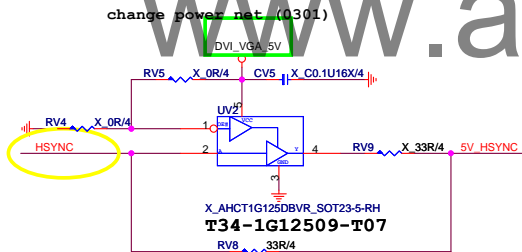
12V - 2.1A
VCC3 - 3A
3VSBV - 375mA



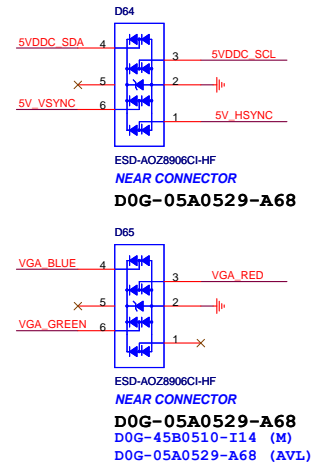
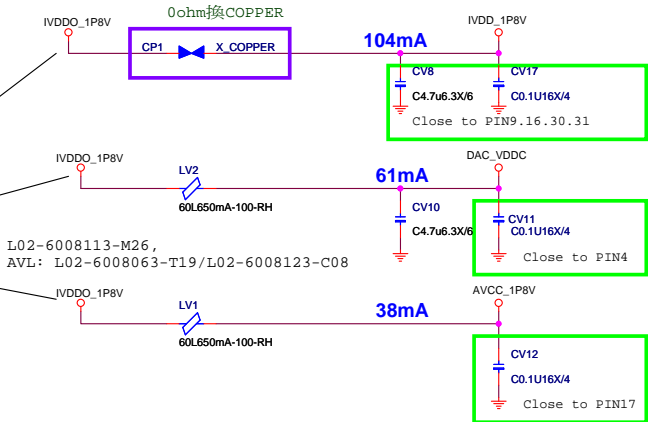
Note:
If connect to eDP port,must confirm whether it support hot plug detection HPD and re-auxtraining



System Status	GPIO	IT6516b's HPD
Legacy Mode (VBIOS) /DOS Mode	HIGH	Force HIGH
Windows /UEFI Mode (GOP)	LOW	Depend on VGA device's plug/unplug

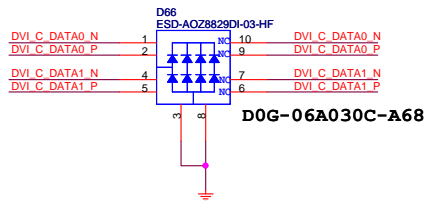
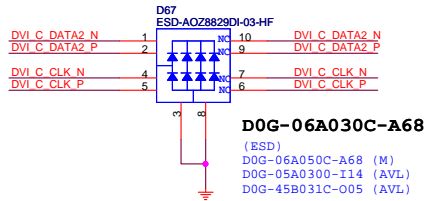
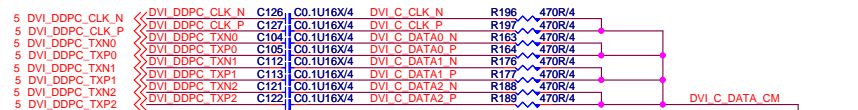


add D-sub function 0225

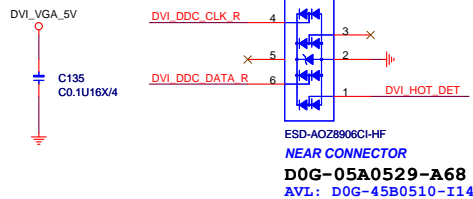


MICRO-STAR INT'L CO.,LTD			
MS-7B61			
Size	Document Description	Rev	
Custom	VGA - ITE6516	1.0	
Date: Wednesday, July 19, 2017	Sheet 22	of 65	

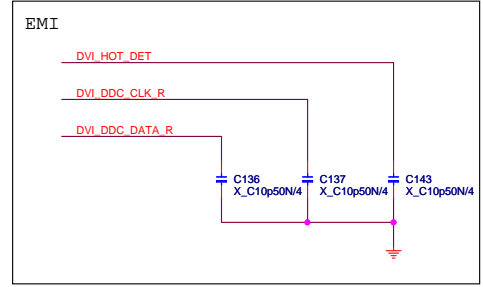
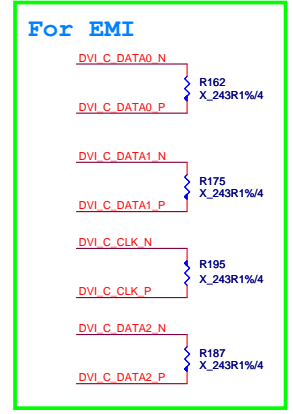
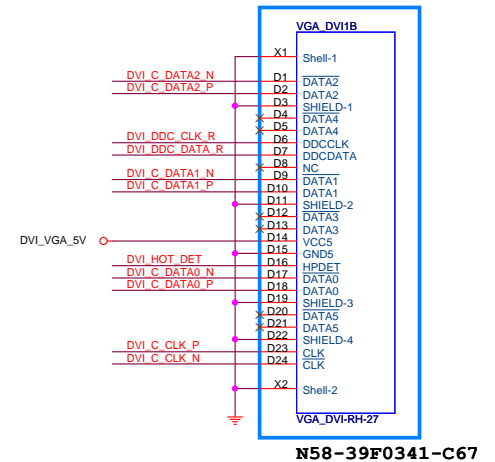
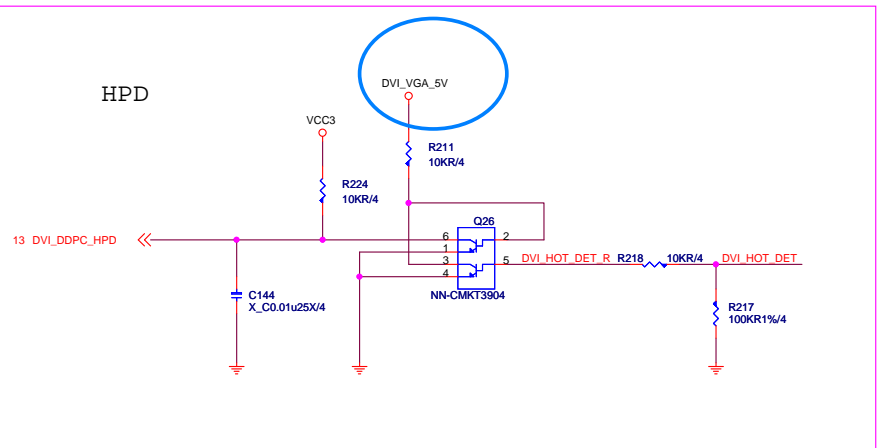
VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)



EMI Cap near connector DV11



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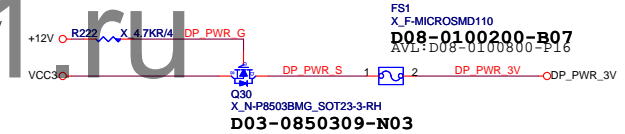
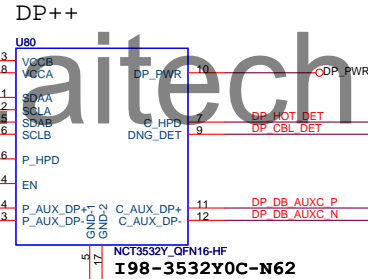
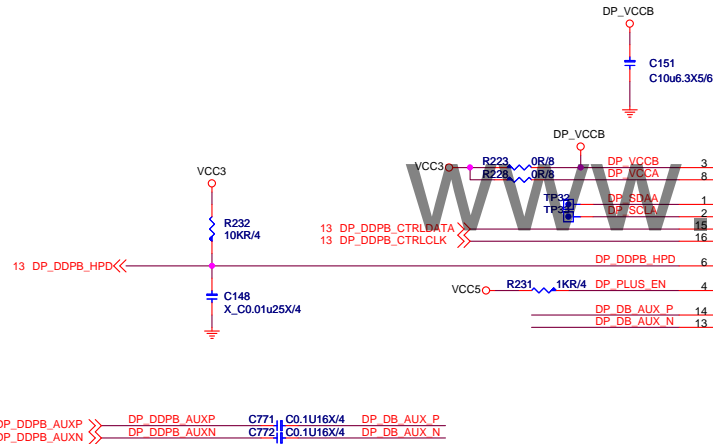
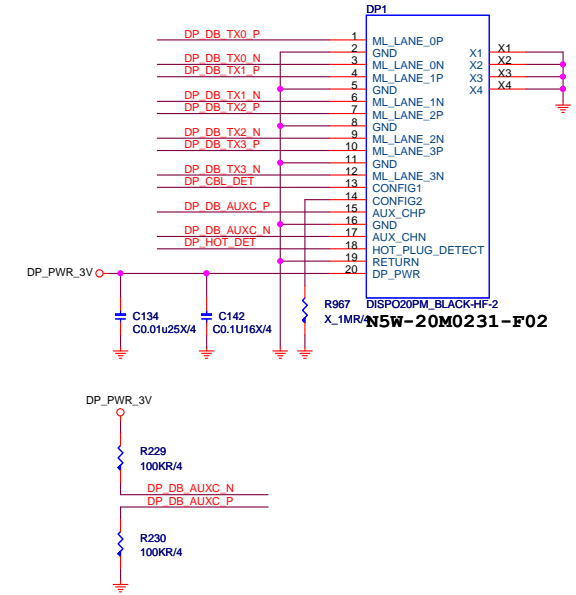
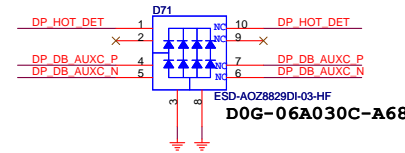
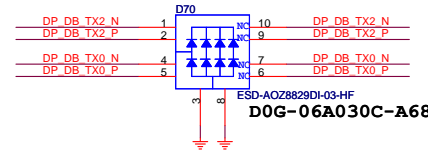
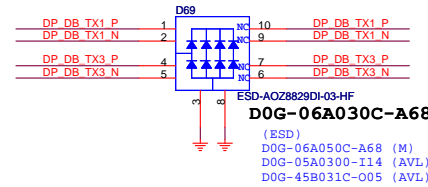
DISPLAY PORT : 1920x1200 at 60 Hz (16:10 WUXGA)

5 DP_DDPB_TX2_P >> DP_DDPB_TX2_P C169 C0.1U16X/4 DP_DB_TX2_P
5 DP_DDPB_TX2_N >> DP_DDPB_TX2_N C163 C0.1U16X/4 DP_DB_TX2_N

5 DP_DDPB_TX1_P >> DP_DDPB_TX1_P C170 C0.1U16X/4 DP_DB_TX1_P
5 DP_DDPB_TX1_N >> DP_DDPB_TX1_N C171 C0.1U16X/4 DP_DB_TX1_N

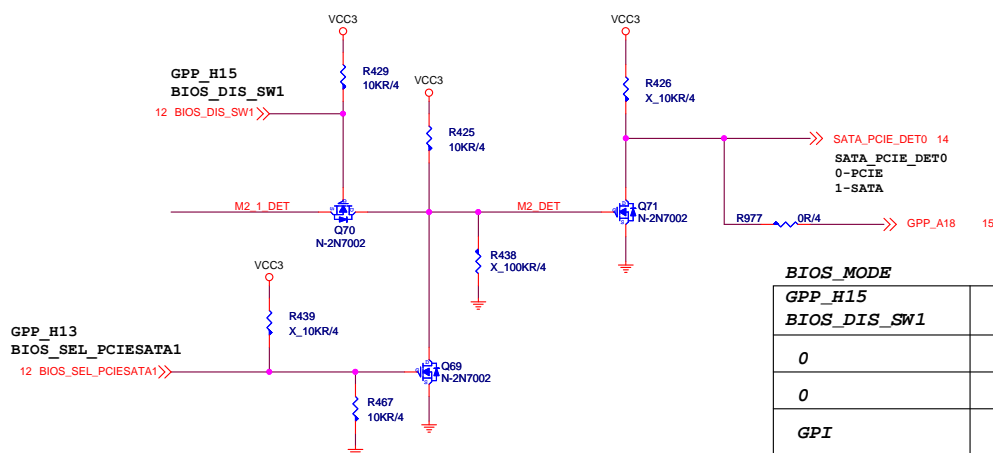
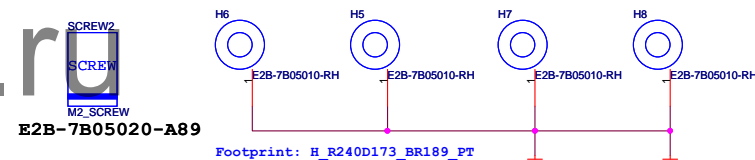
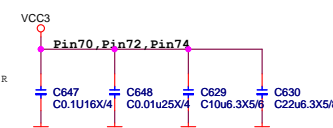
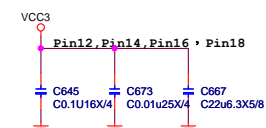
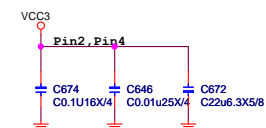
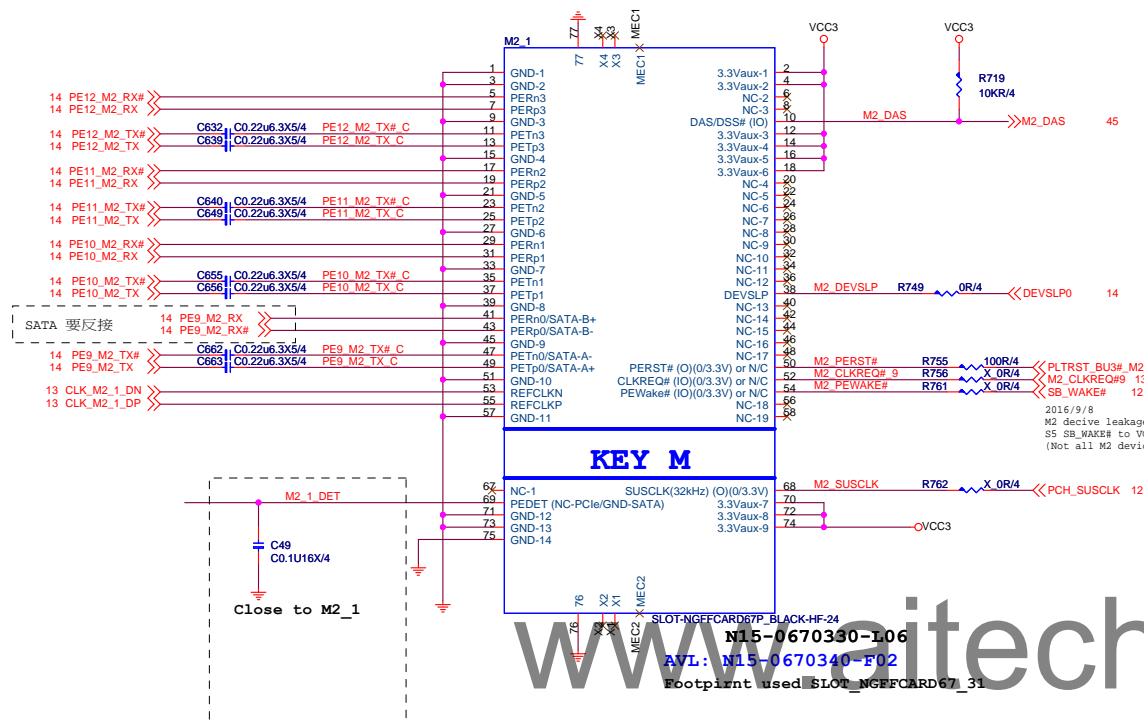
5 DP_DDPB_TX0_P >> DP_DDPB_TX0_P C162 C0.1U16X/4 DP_DB_TX0_P
5 DP_DDPB_TX0_N >> DP_DDPB_TX0_N C159 C0.1U16X/4 DP_DB_TX0_N

5 DP_DDPB_TX3_P >> DP_DDPB_TX3_P C178 C0.1U16X/4 DP_DB_TX3_P
5 DP_DDPB_TX3_N >> DP_DDPB_TX3_N C179 C0.1U16X/4 DP_DB_TX3_N

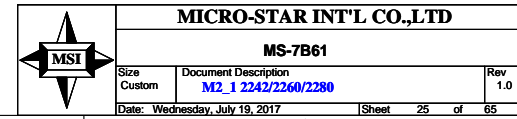


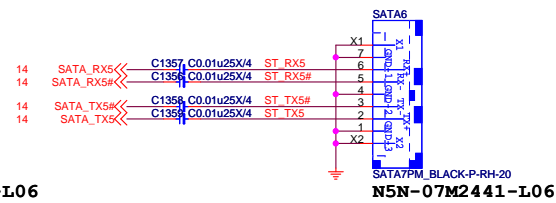
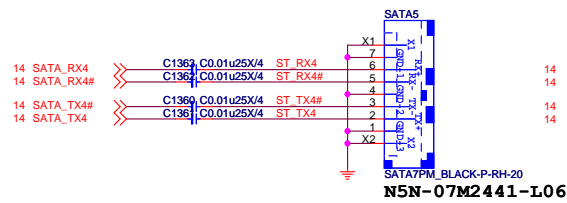
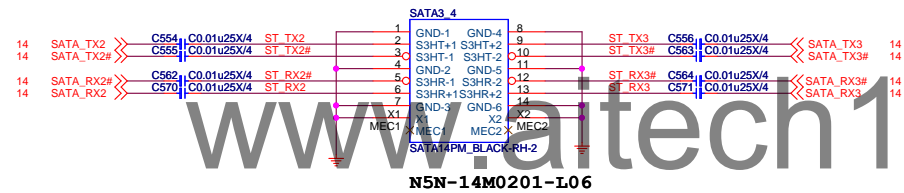
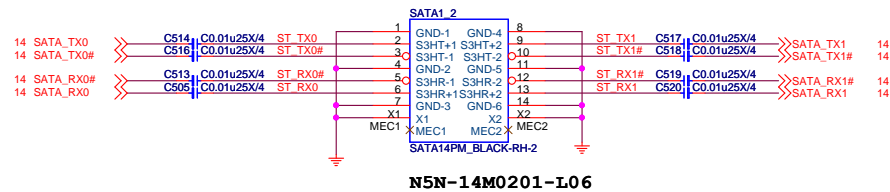
5 DP_DDPB_AUXP >> DP_DDPB_AUXP C771 C0.1U16X/4 DP_DB_AUX_P
5 DP_DDPB_AUXN >> DP_DDPB_AUXN C772 C0.1U16X/4 DP_DB_AUX_N

M2_1 2242/2260/2280/22110
(PCIeX4 mode and SATA mode)



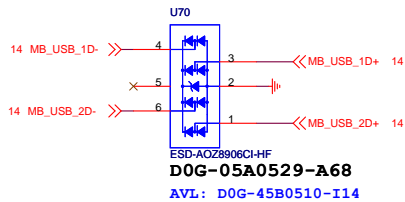
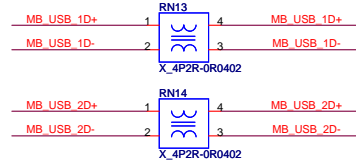
BIOS_MODE		
GPP_H15 BIOS_DIS_SW1	GPP_H13 BIOS_SEL_PCIESATA1	
0	1	M2-SATA
0	0	M2-PCIE X4
GPI	GPI	AUTO



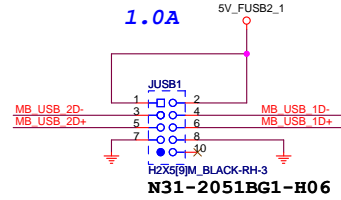


FRONT USB2.0 PORT 1,2

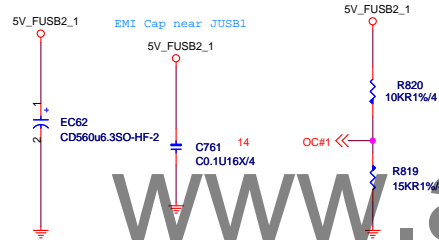
ComChoke co-lay 4P2R-0R0402
Footprint: FILTER_S4_RN4P2R_COLAY
Defaule ComChoke: L12-9008080-P01
4P2R-0R0402: R3C-0000012-W08



ESD-AOZ8906CI-HF
D0G-05A0529-A68
AVL: D0G-45B0510-I14



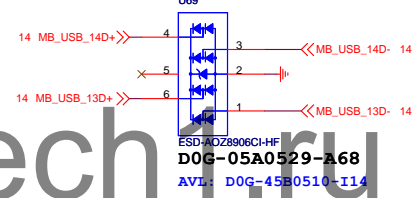
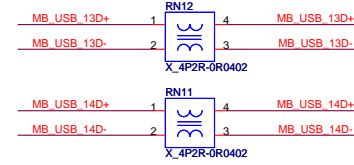
H2X5[9]M_BLACK-RH-3
N31-2051BG1-H06



C71-5610671-N07

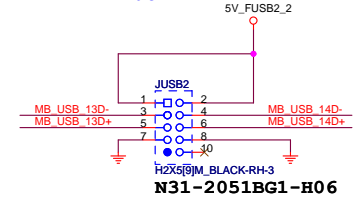
FRONT USB2.0 PORT 13,14 (Z270 only)

ComChoke co-lay 4P2R-0R0402
Footprint: FILTER_S4_RN4P2R_COLAY
Defaule ComChoke: L12-9008080-P01
4P2R-0R0402: R3C-0000012-W08

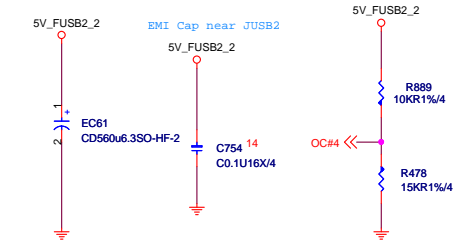


ESD-AOZ8906CI-HF
D0G-05A0529-A68
AVL: D0G-45B0510-I14

1.0A



H2X5[9]M_BLACK-RH-3
N31-2051BG1-H06



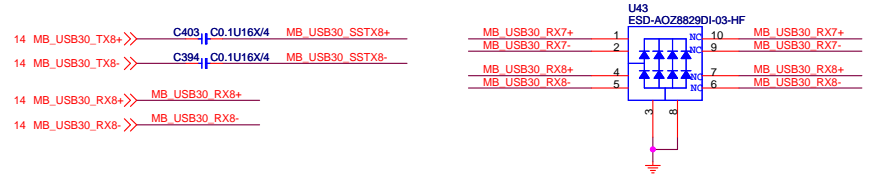
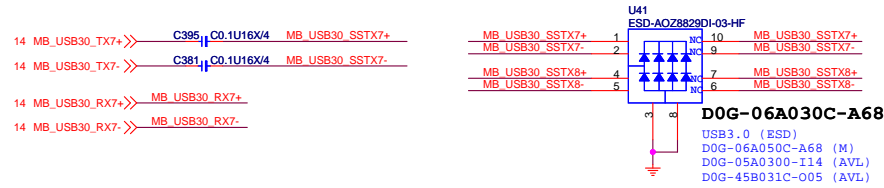
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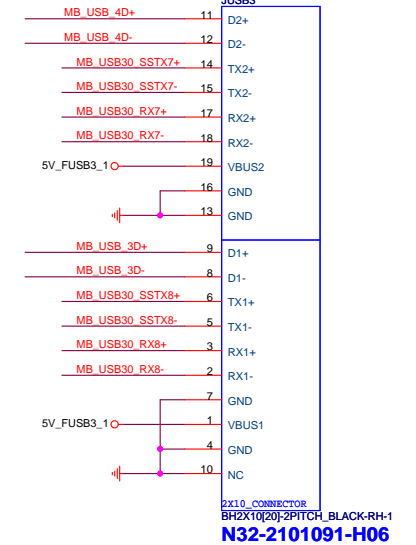
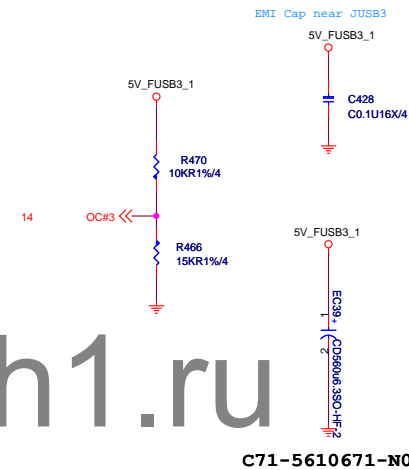
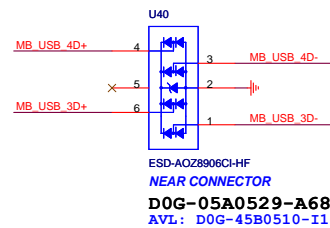
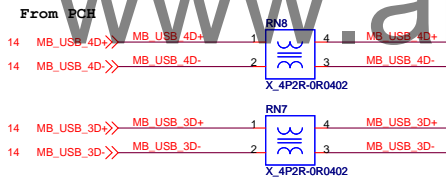
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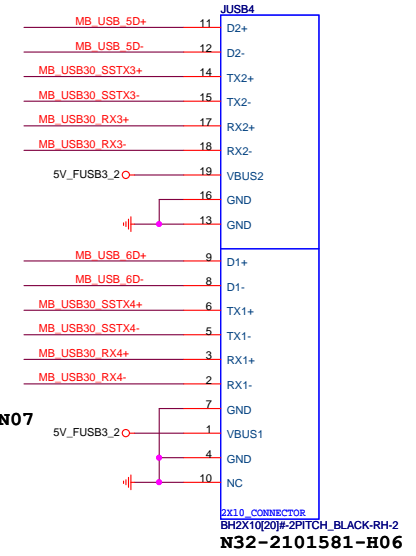
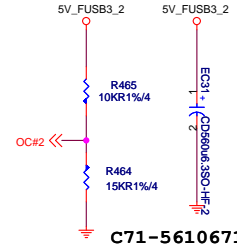
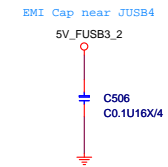
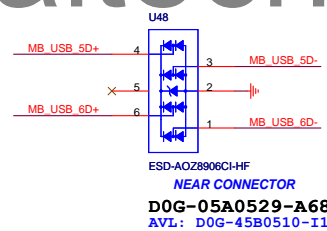
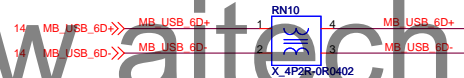
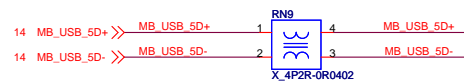
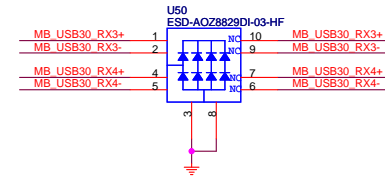
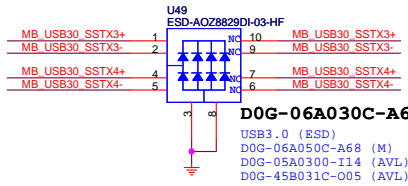
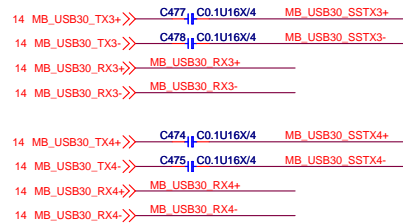
MS-7B61

Size	Document Description	Rev
Custom	Front USB2	1.0
Date: Wednesday, July 19, 2017	Sheet 28 of 65	



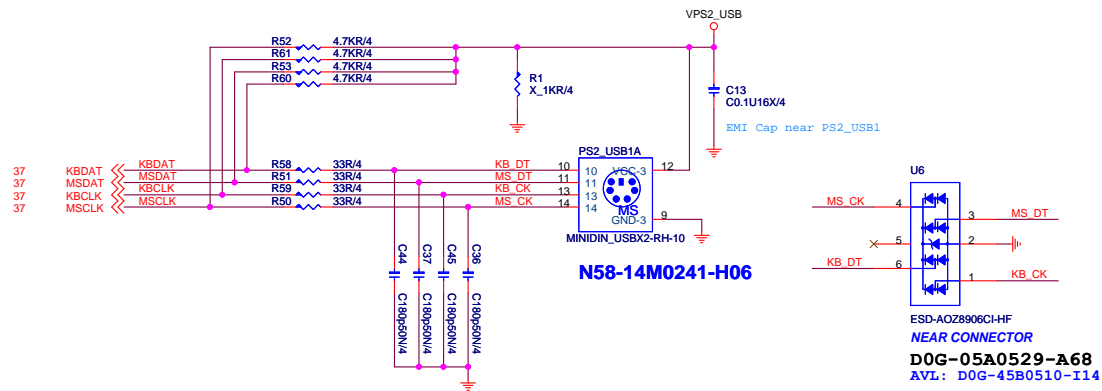
ComChoke co-lay 4P2R-0R0402
 Footprint: FILTER_S4_RN4P2R_COLAY
 Defaule ComChoke: L12-9008080-P01
 4P2R-0R0402: R3C-0000012-008



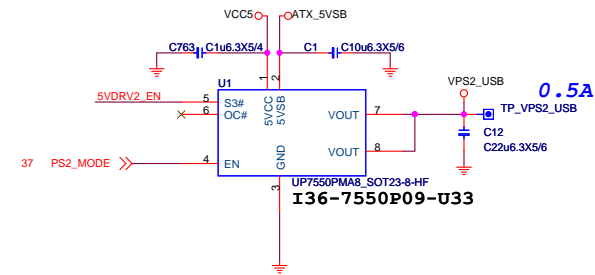


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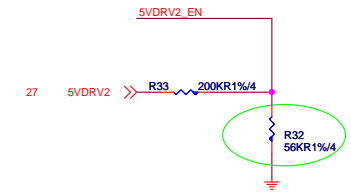
PS2 KEYBOARD & MOUSE CONNECTOR



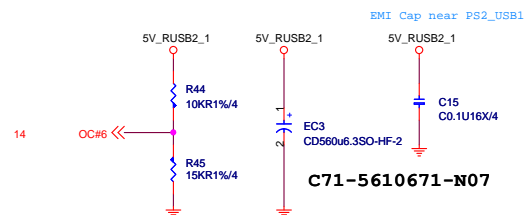
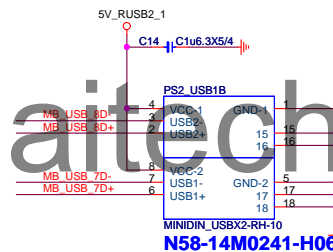
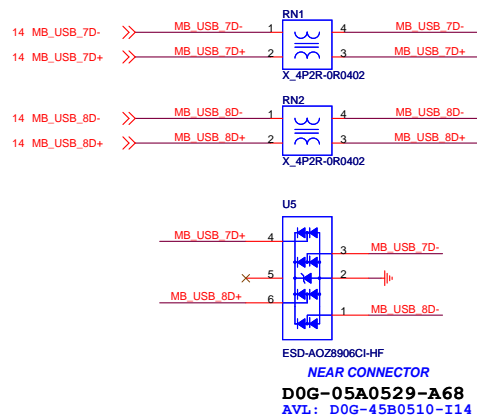
PS2 Power



USB MODE



ComChoke co-lay 4P2R-0R0402
Footprint: FILTER_S4_RN4P2R_COLAY
Defaule ComChoke: L12-9008080-P01
4P2R-0R0402: R3C-0000012-W08



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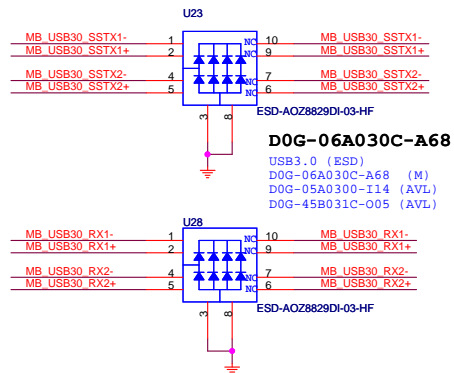
Size	Document Description	Rev
Custom	Rear PS2_USB1	1.0
Date: Wednesday, July 19, 2017	Sheet 31 of 65	

14 MB_USB30_TX1+ >>> C187 C0.1U16X/4 MB_USB30_SSTX1+
14 MB_USB30_TX1- >>> C188 C0.1U16X/4 MB_USB30_SSTX1-

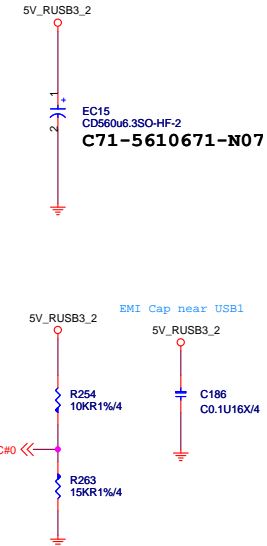
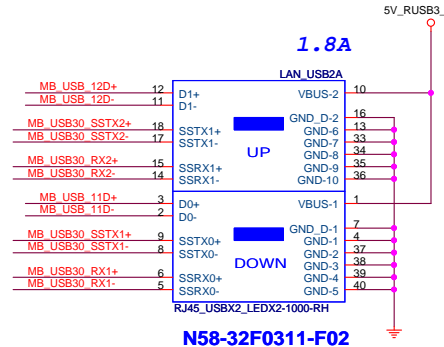
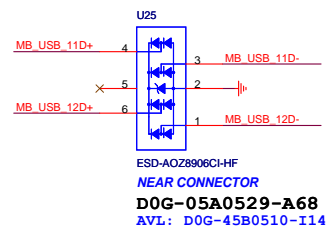
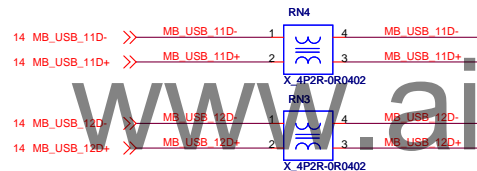
14 MB_USB30_RX1+ >>> MB_USB30_RX1+
14 MB_USB30_RX1- >>> MB_USB30_RX1-

14 MB_USB30_TX2+ >>> C203 C0.1U16X/4 MB_USB30_SSTX2+
14 MB_USB30_TX2- >>> C204 C0.1U16X/4 MB_USB30_SSTX2-

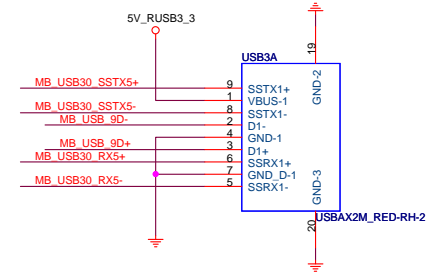
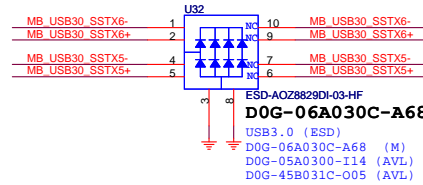
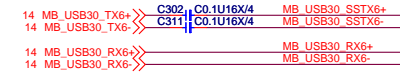
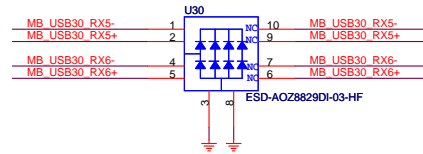
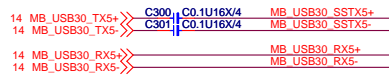
14 MB_USB30_RX2+ >>> MB_USB30_RX2+
14 MB_USB30_RX2- >>> MB_USB30_RX2-



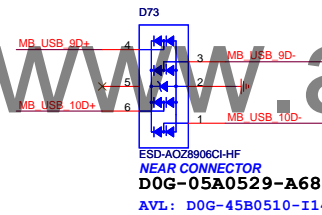
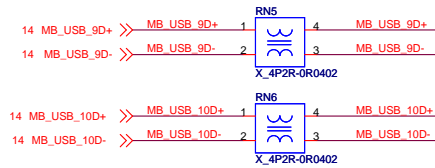
ComChoke co-lay 4P2R-0R0402
Footprint: FILTER_S4_RN4P2R_COLAY
Defaule ComChoke: L12-9008080-P01
4P2R-0R0402: R3C-0000012-W08



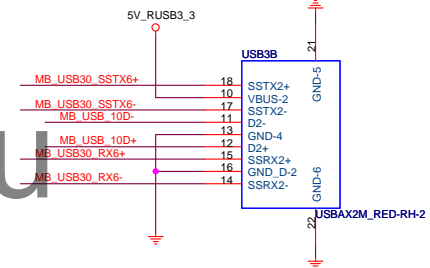
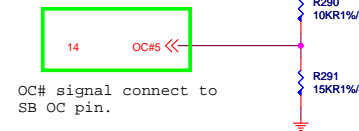
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N53-18M0201-L06

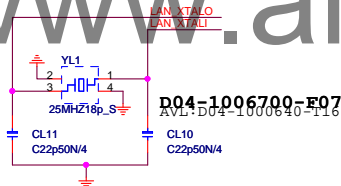
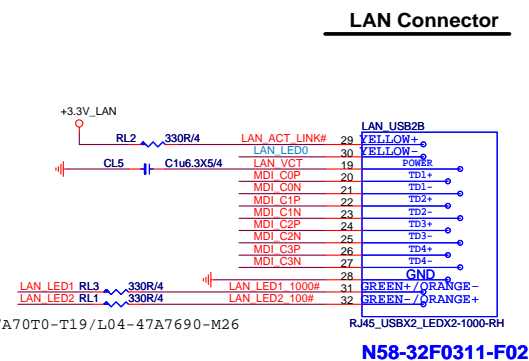


C71-5610671-N07

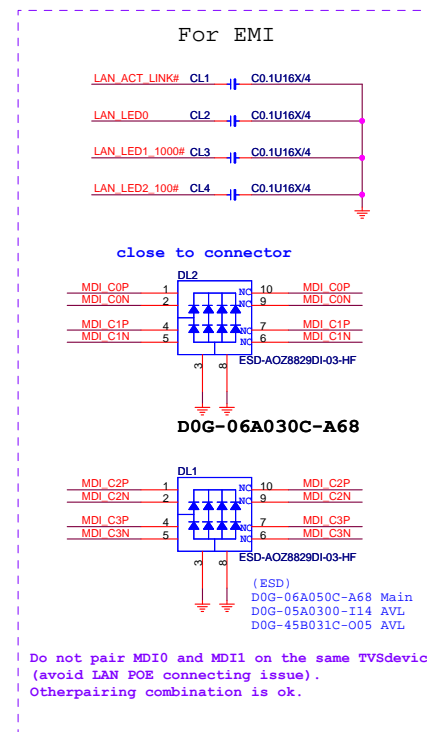


N53-18M0201-L06

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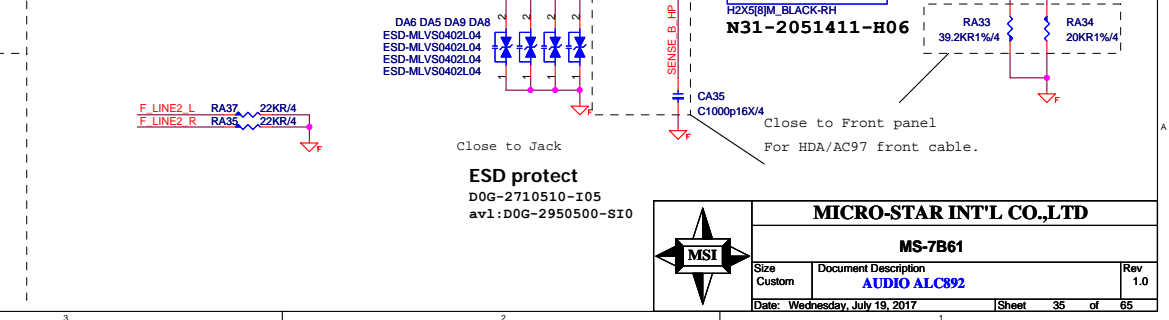
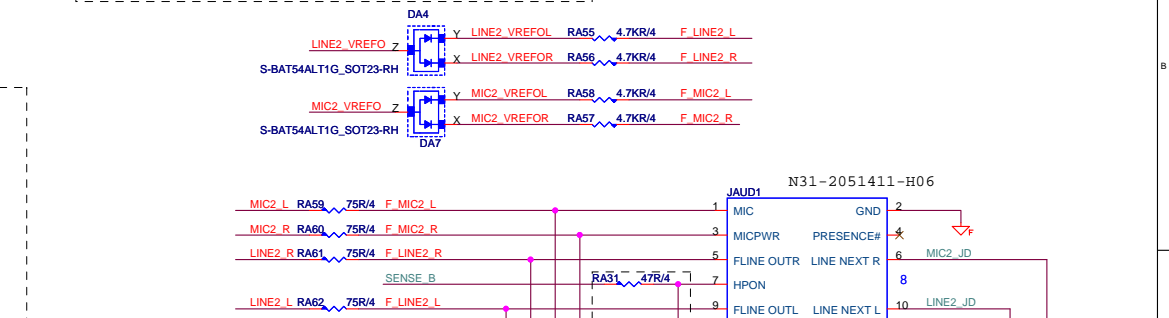
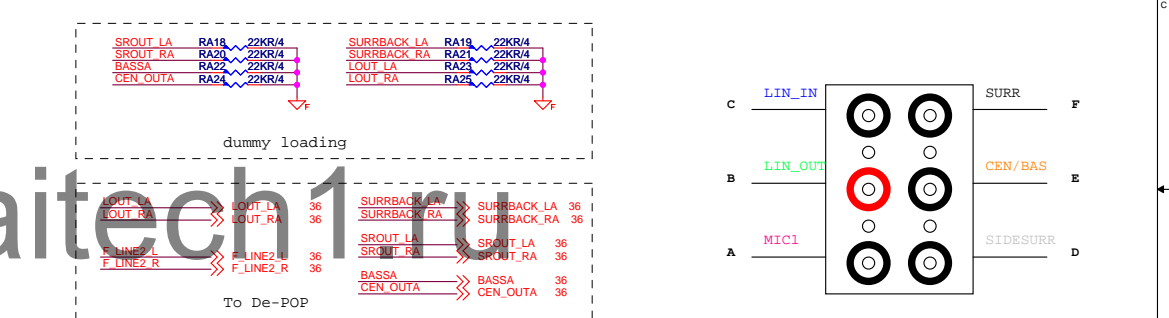
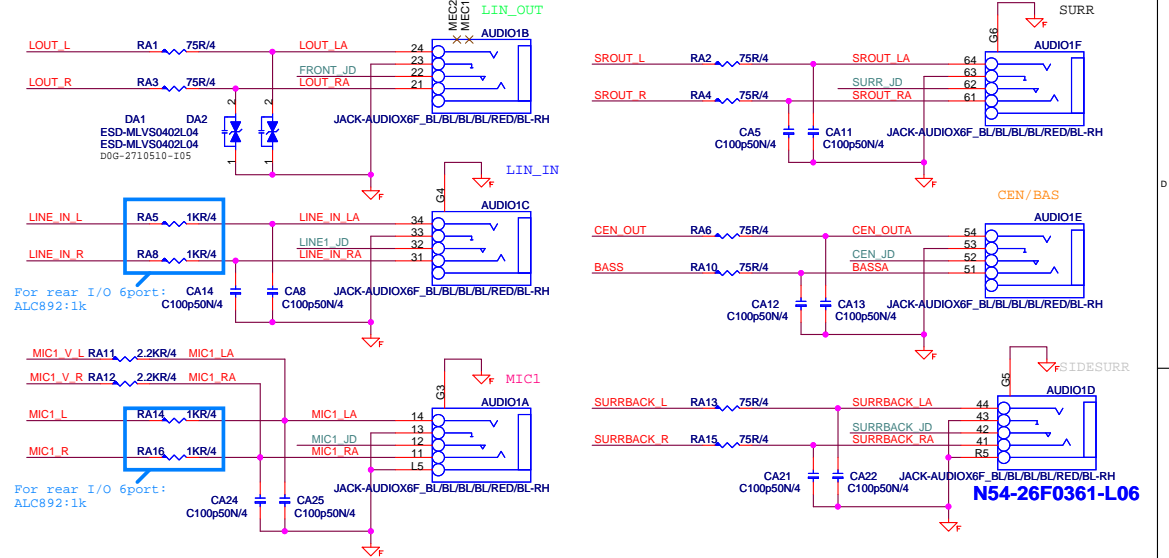
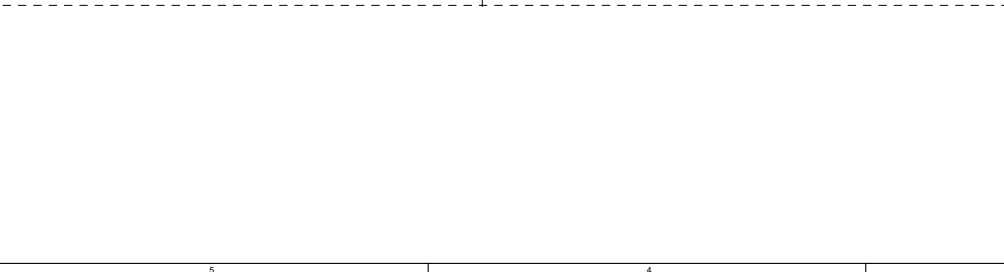
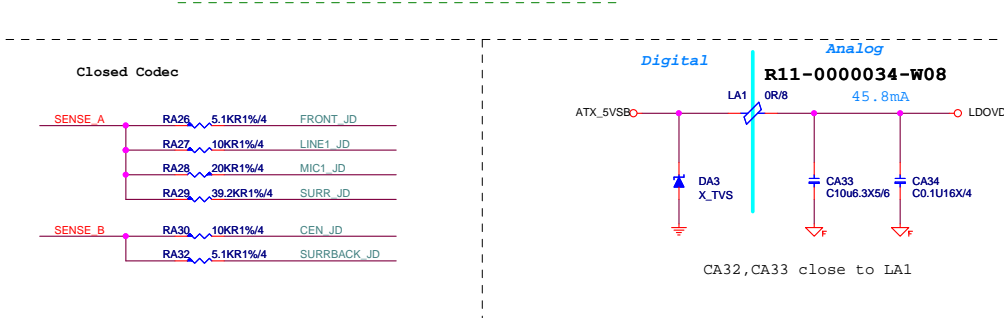
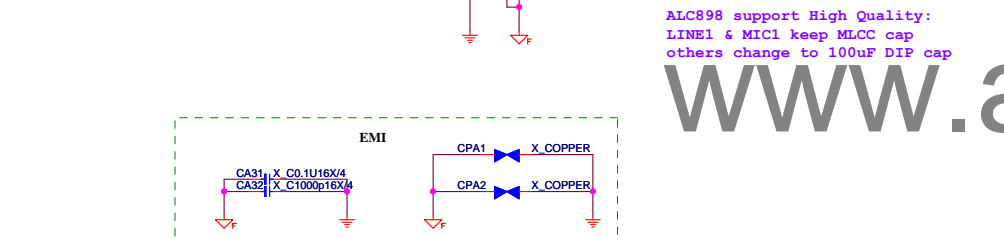
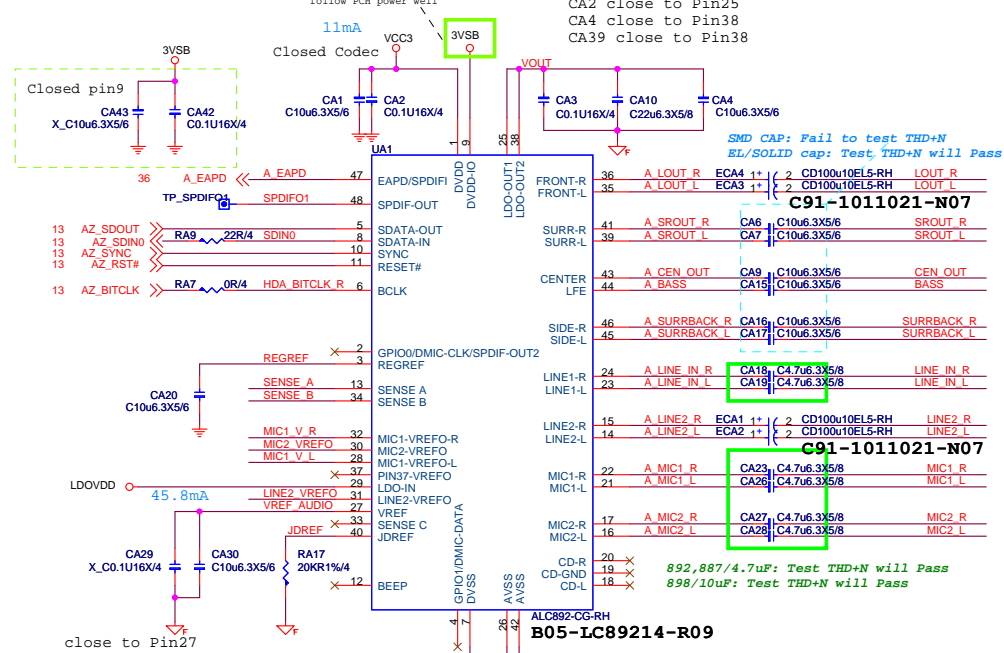


Power source from 3VA (DSW power) & make sure MAX current is enough to support i218/i219.



	MICRO-STAR INT'L CO.,LTD		
	MS-7B61		
	Size Custom	Document Description LAN-RTL811H	Rev 1.0
	Date: Wednesday, July 19, 2017		Sheet 34 of 65

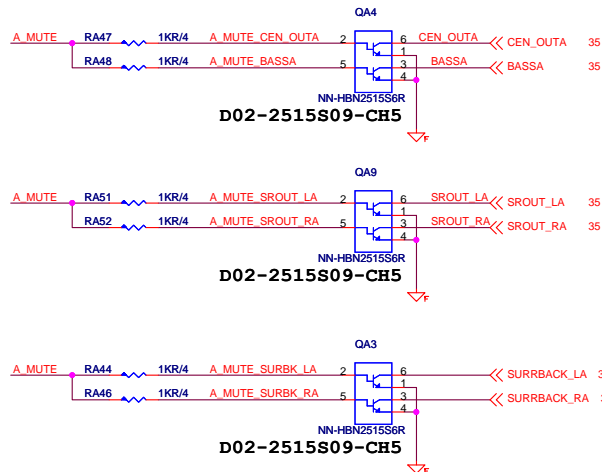
ALC892 Type A:



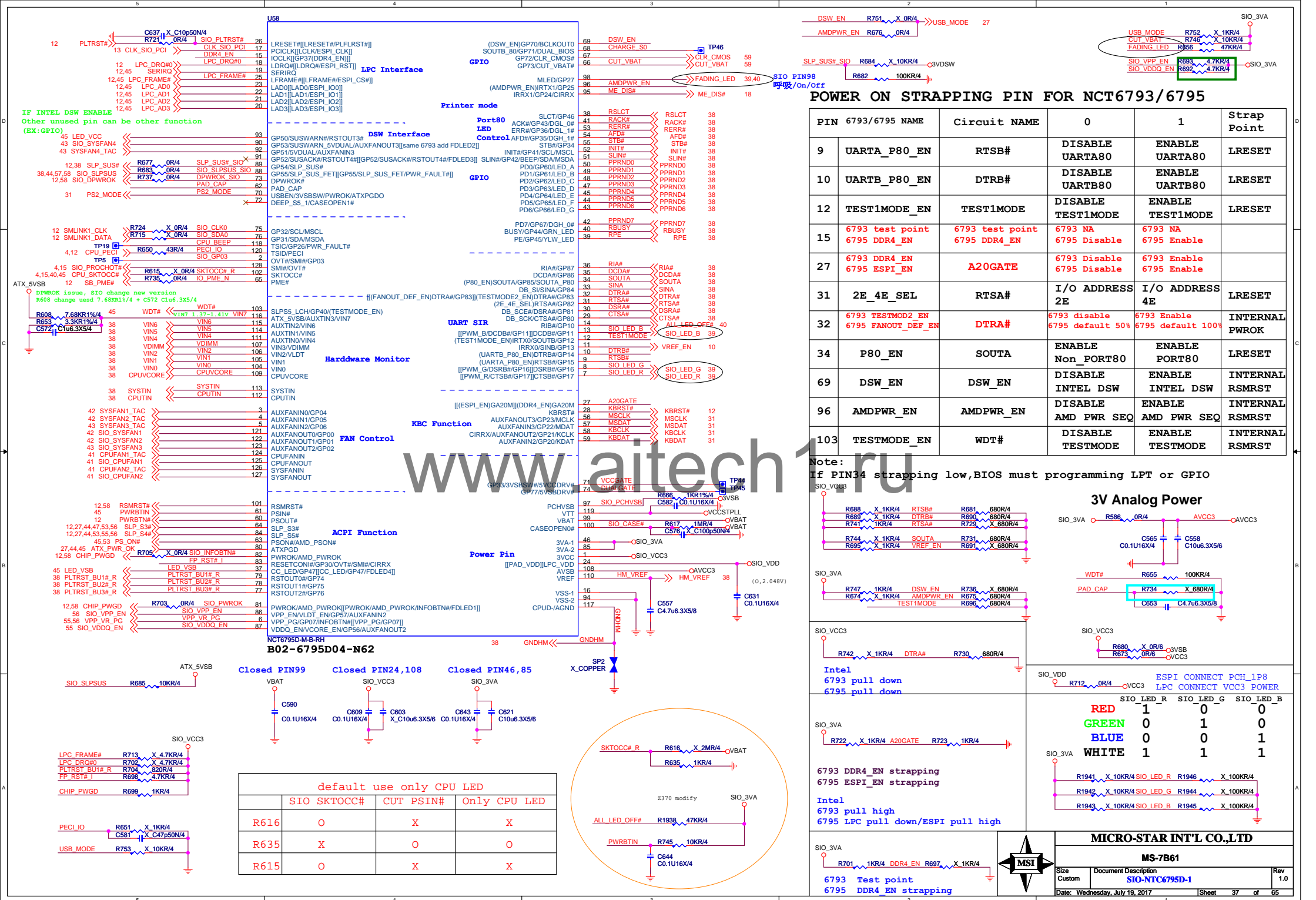
www.aitech1.com

(De-pop circuit for Rear Line out & Front Headphone out)

www.aitech1.ru



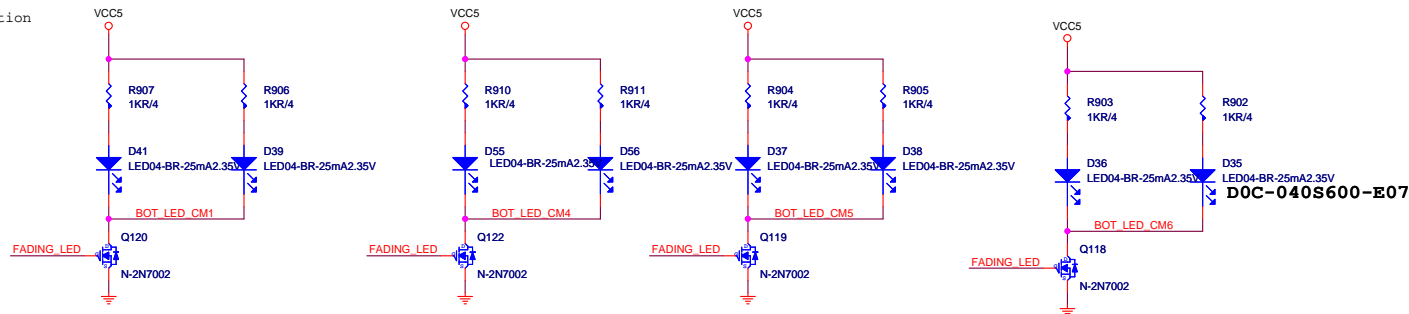
2015/11/09:
esd p/n m:D0G-2710510-I05;avl:D0G-2950500-SI0



BOTTOM LED

PCB bottom side Screw holes
LED White : D0C-040T300-H91 * 8pcs

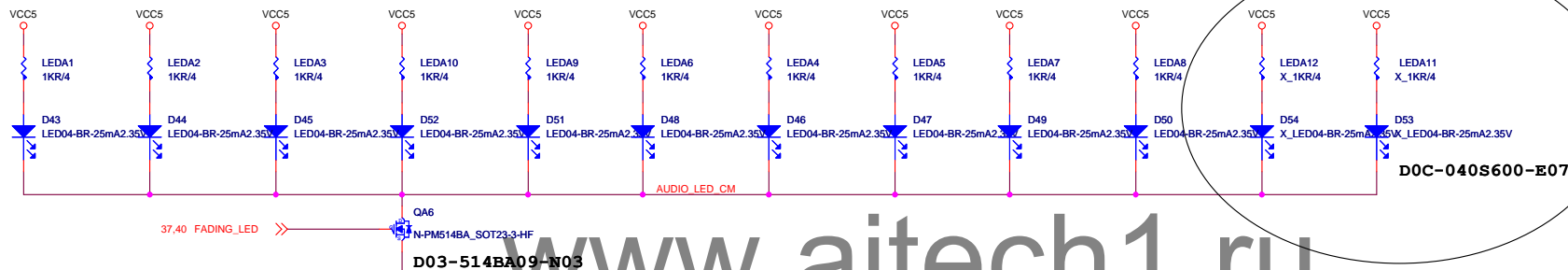
2016.08. 22 Remove Bottom LED function



AUDIO LED

Audio Moat Line LED Red :
LED RED : D0C-040S600-E07 * 12pcs

Audio moat is transparent and width 40mil



JLED1 RGB LED CONTROL

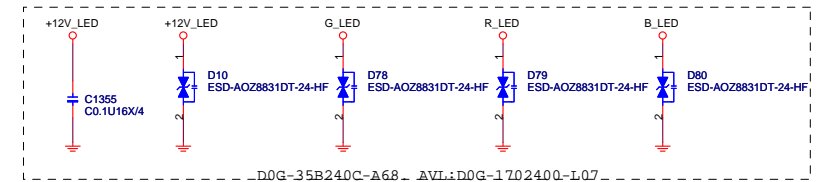
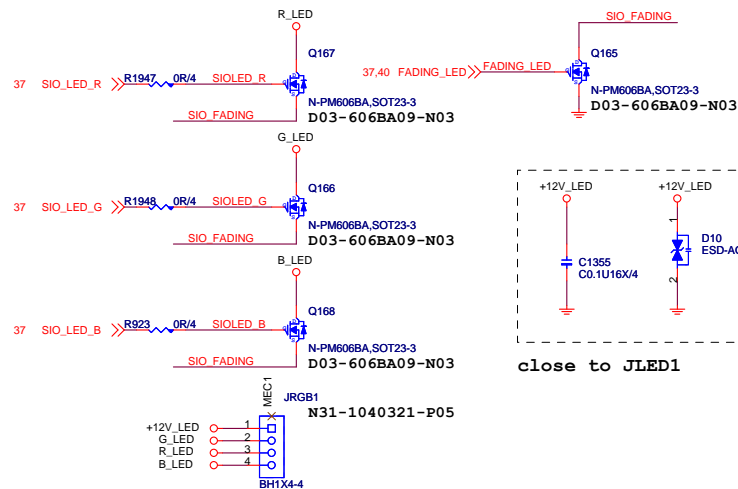
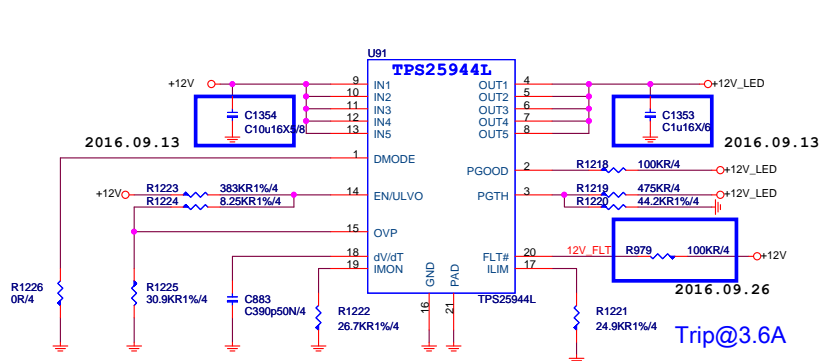
定義: 外接LED 燈條

---- 彩色 : SIO 6795D-M(128pin) : OB2-7A58001

---- 單色 : SIO 5565(64pin) : B02-5565D04-N62

---- PCB 文字面 (JLED)

---- 手冊 註明接頭支援標準 5050 RGB or 單色 LED 共陽燈條 (12V+/G/R/B) or (12V+/-/S/-) , 燈條總輸出電流限制為3安培 (12 伏特) , 長度限制為2公尺

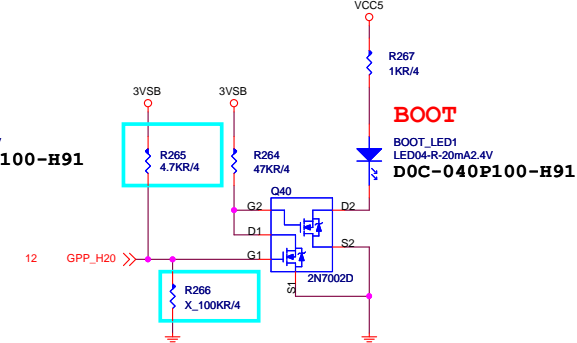
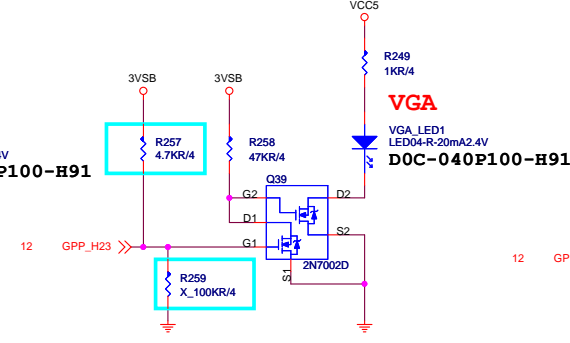
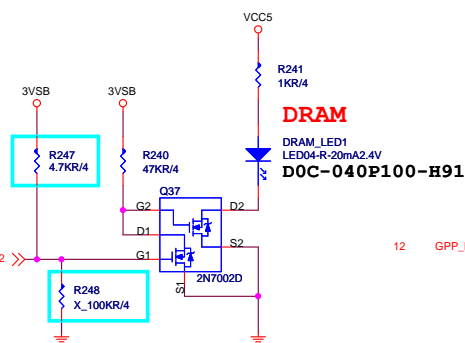
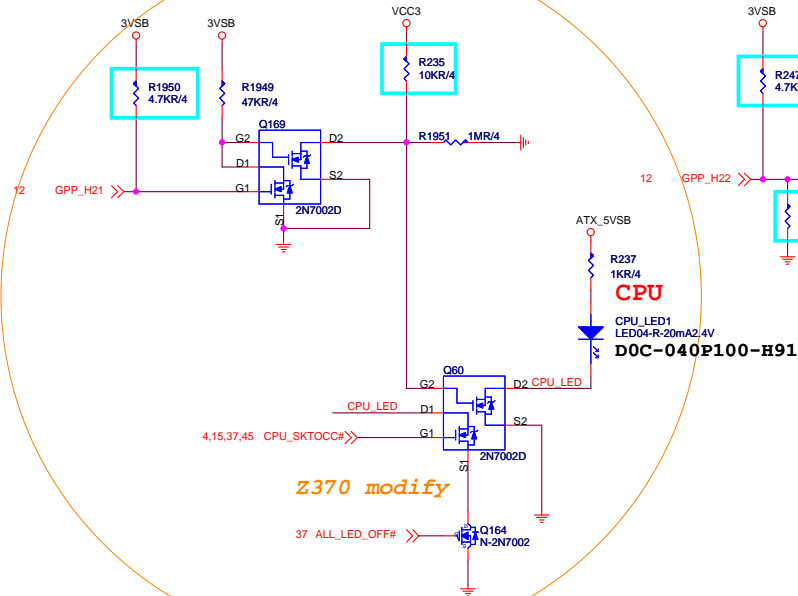


close to JLED1

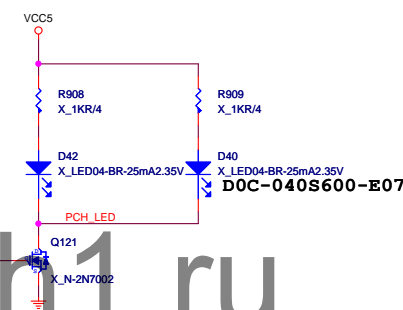
MICRO-STAR INT'L CO.,LTD			
MS-7B61			
Size	Document Description	Rev	
Custom	LED-BOT/AUD/LBAR	1.0	
Date:	Wednesday, July 19, 2017	Sheet	39 of 65

EZ Debug

EZ Debug LED RED
M:D0C-040P100-H91



PCH_LED

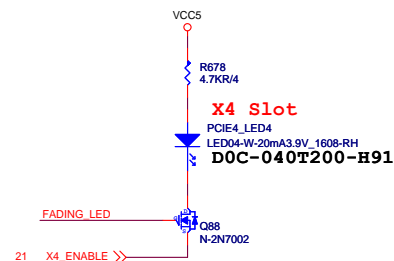
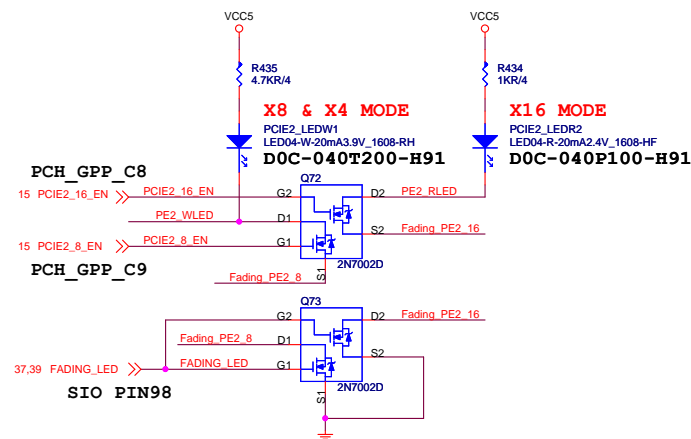


PCIE

PCIE SLOT LED

PCIE SLOT LED 命名請以PCIE LEDn n為數字
PCIE x16 紅 : M:D0C-040P100-H91 / S:D0C-040S500-E07
PCIE x4 白 : D0C-040T200-H91 / S:D0C-040S200-E07
PCIE x1 白 : D0C-040T200-H91 / S:D0C-040S200-E07

GPIO LED	GPP_C8	GPP_C9
亮	GPO PO HIGH	GPO PO HIGH
滅	GPI (default LOW)	GPI (default LOW)



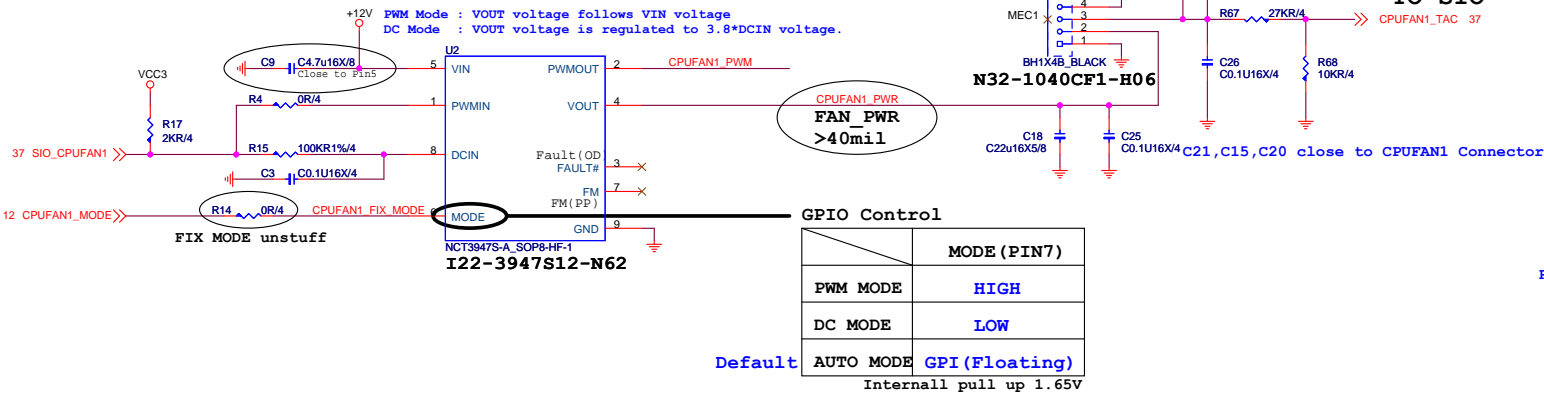
MICRO-STAR INT'L CO.,LTD

MS-7B61

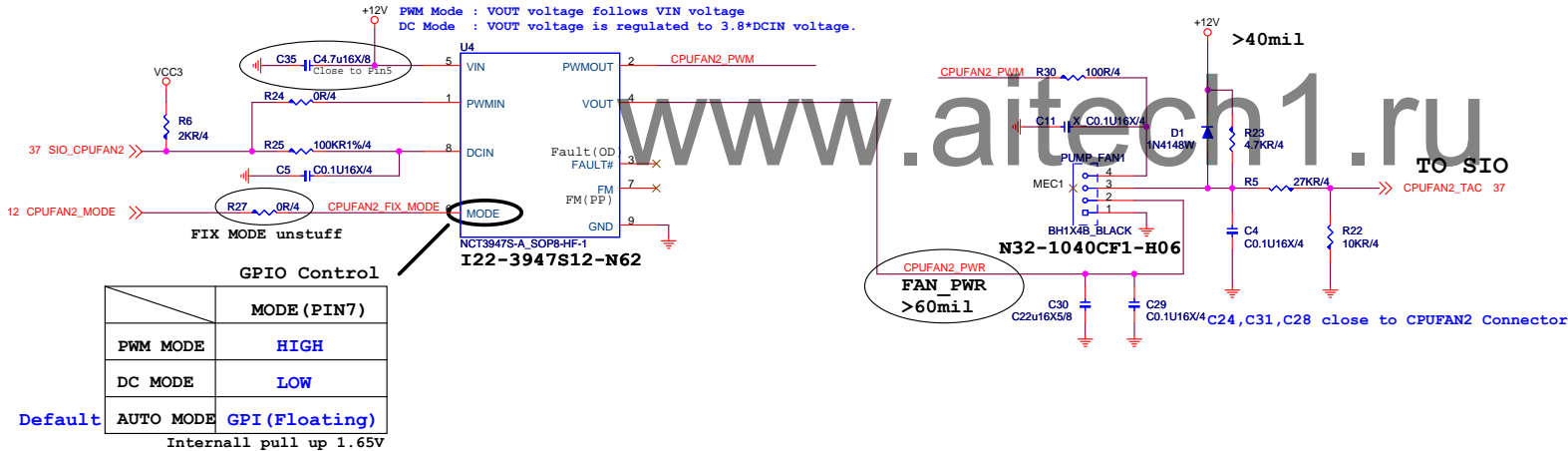
Size	Document Description	Rev
Custom	LED-EZ DBG/DIMM/PCIE	1.0
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TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

- 1. PWM/DC/OCF LED (現在是改成R/G/B3色LED)
- 2. GPIO可以由BIOS切換 PWM/DC MODE
- 3. OCP拉回GPIO給BIOS認
- 4. PWM OR DC FAN拉回GPIO給BIOS認
- 5. FAN轉速加快的時候由SOFTWARE 控制GPIO讓燈的變化

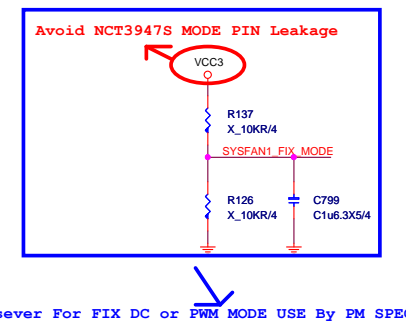


TYPEK : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE (2A pump FAN)

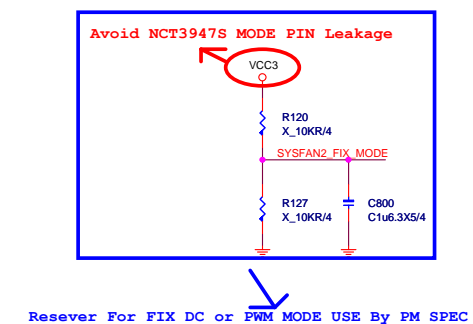


- 1. MODE : USE MODE PIN change FAN MODE (PWM or DC FAN)
- 2. FAULT : USE FAULT PIN Triger OVT/OCF Protection, LOW Atcive (Reserve NEW IC)
- 3. FM : USE FM PIN For BIOS USE to Detect PWM or DC FAN & Show information (Reserve NEW IC)

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE



Default	AUTO MODE	GPI (Floating)
Internall pull up 1.65V		



	MODE (PIN7)
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI(Floating)

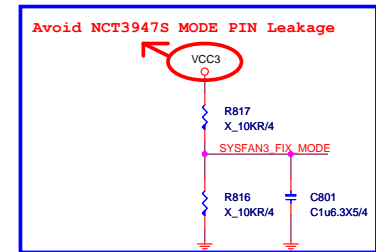
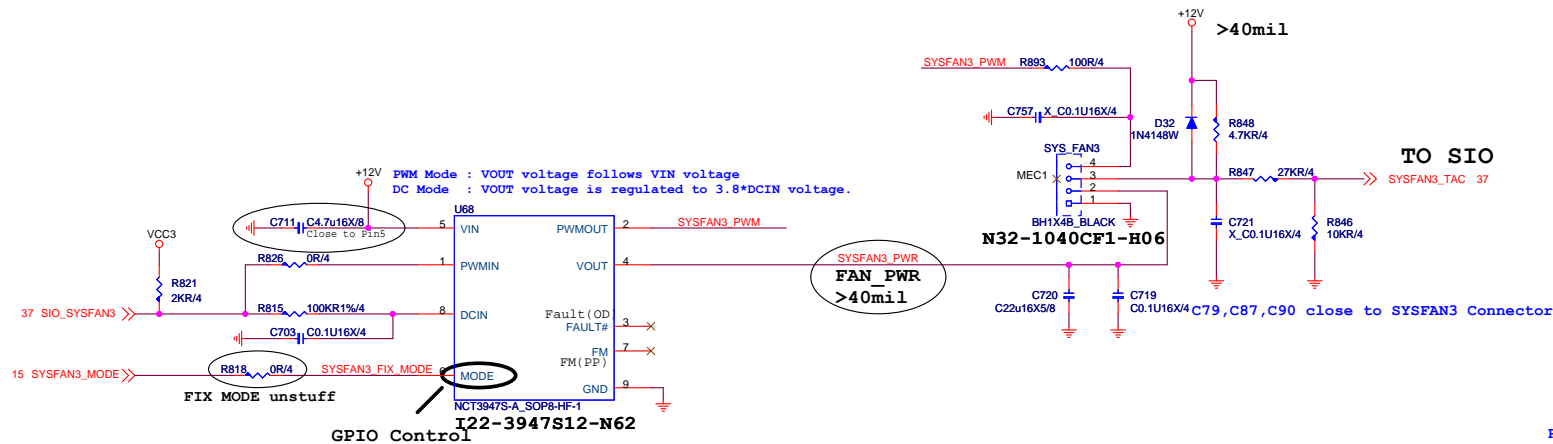
Internall pull up 1.65V



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Size Custom	Document Description SYSTEM FAN 1/2	Rev 1.0
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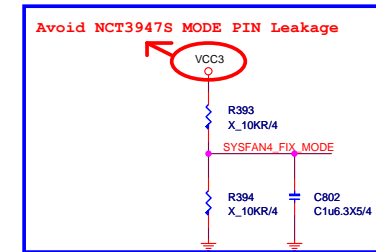
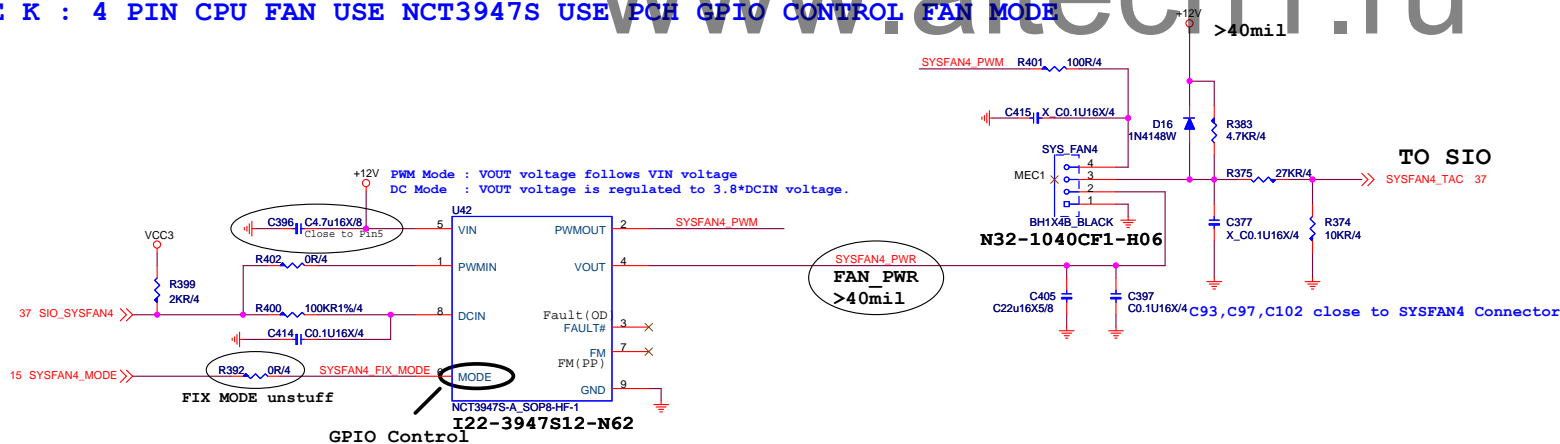
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE



Resever For FIX DC or PWM MODE USE By PM SPEC

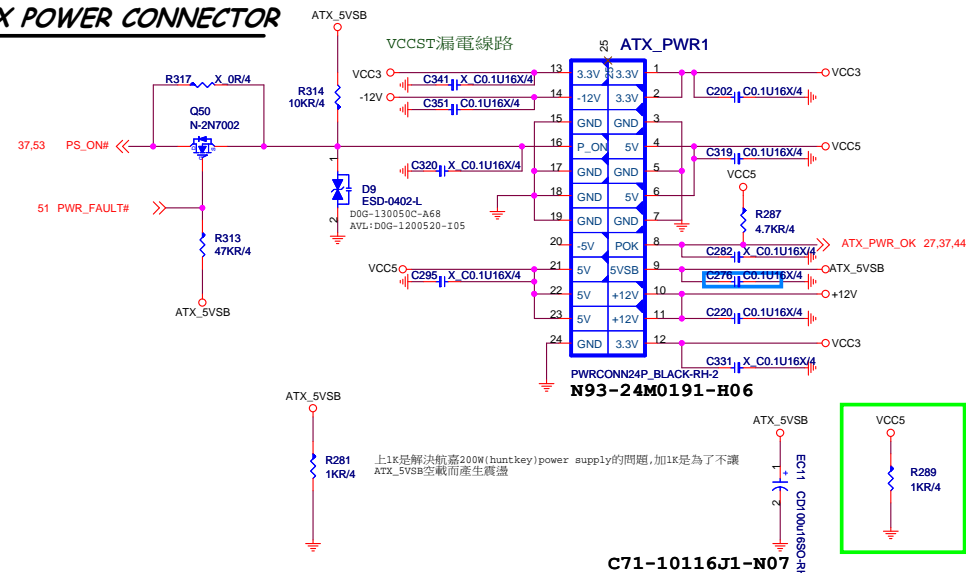
www.aitech1.ru

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

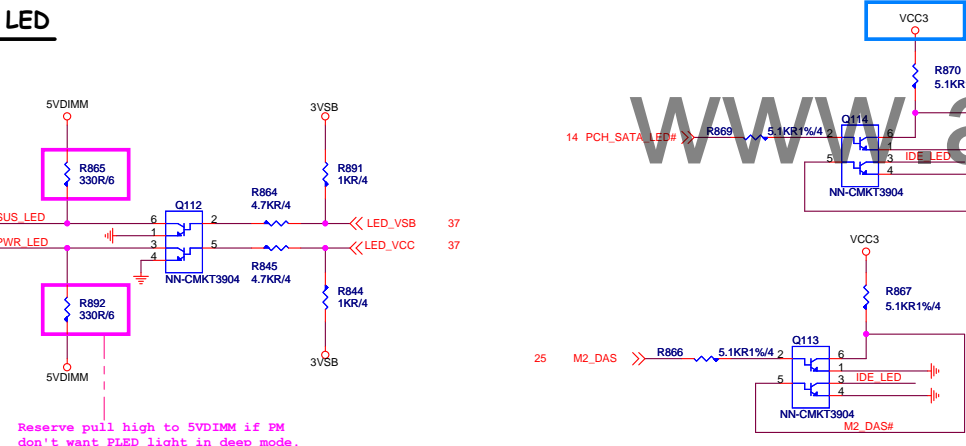


Resever For FIX DC or PWM MODE USE By PM SPEC

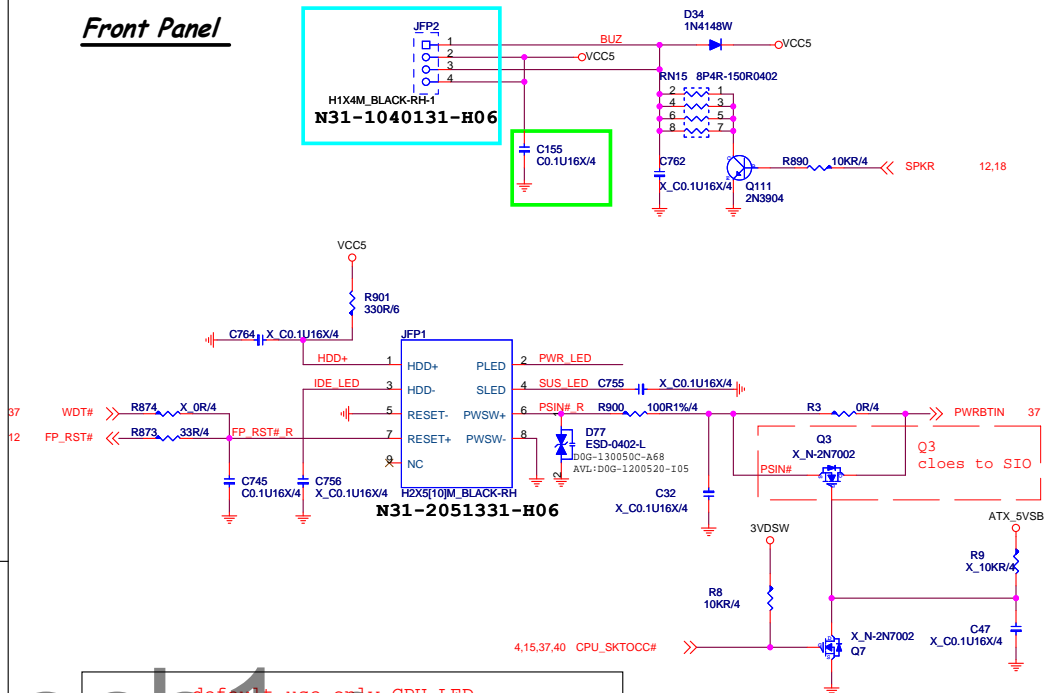
ATX POWER CONNECTOR



LED

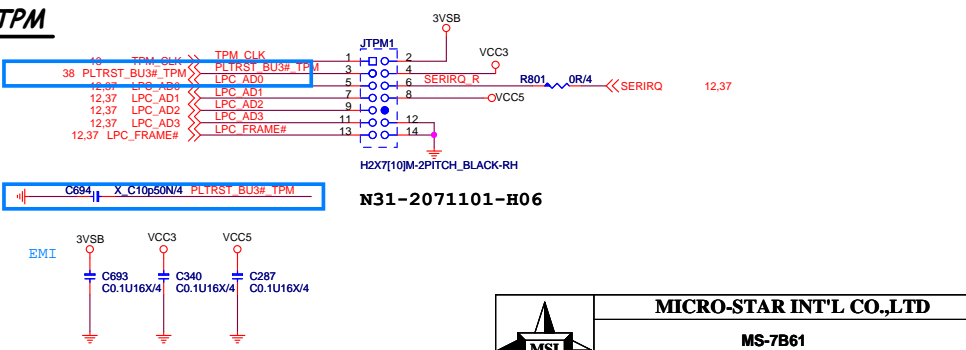


Front Panel



	default use only CPU LED	SIO SKTOCC#	CUT PSIN#	Only CPU LED
R3	O	X		O
Q3	X		O	X
C32	X		O	X
R8	X		O	O
D77	X		O	X
Q7	X		O	X
R9	X		O	X
C47	X	X	X	X

TPM



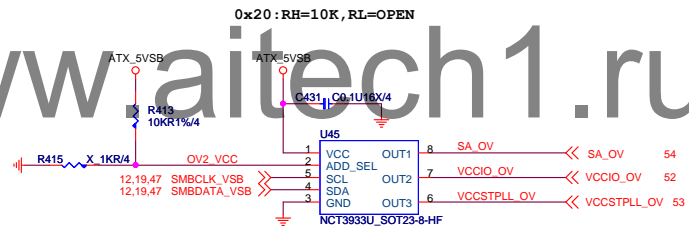
MICRO-STAR INT'L CO.,LTD

MS-7B61


Size	Document Description	Rev
Custom	ATX Power/F_Panel/JTPM/JTBT	1.0

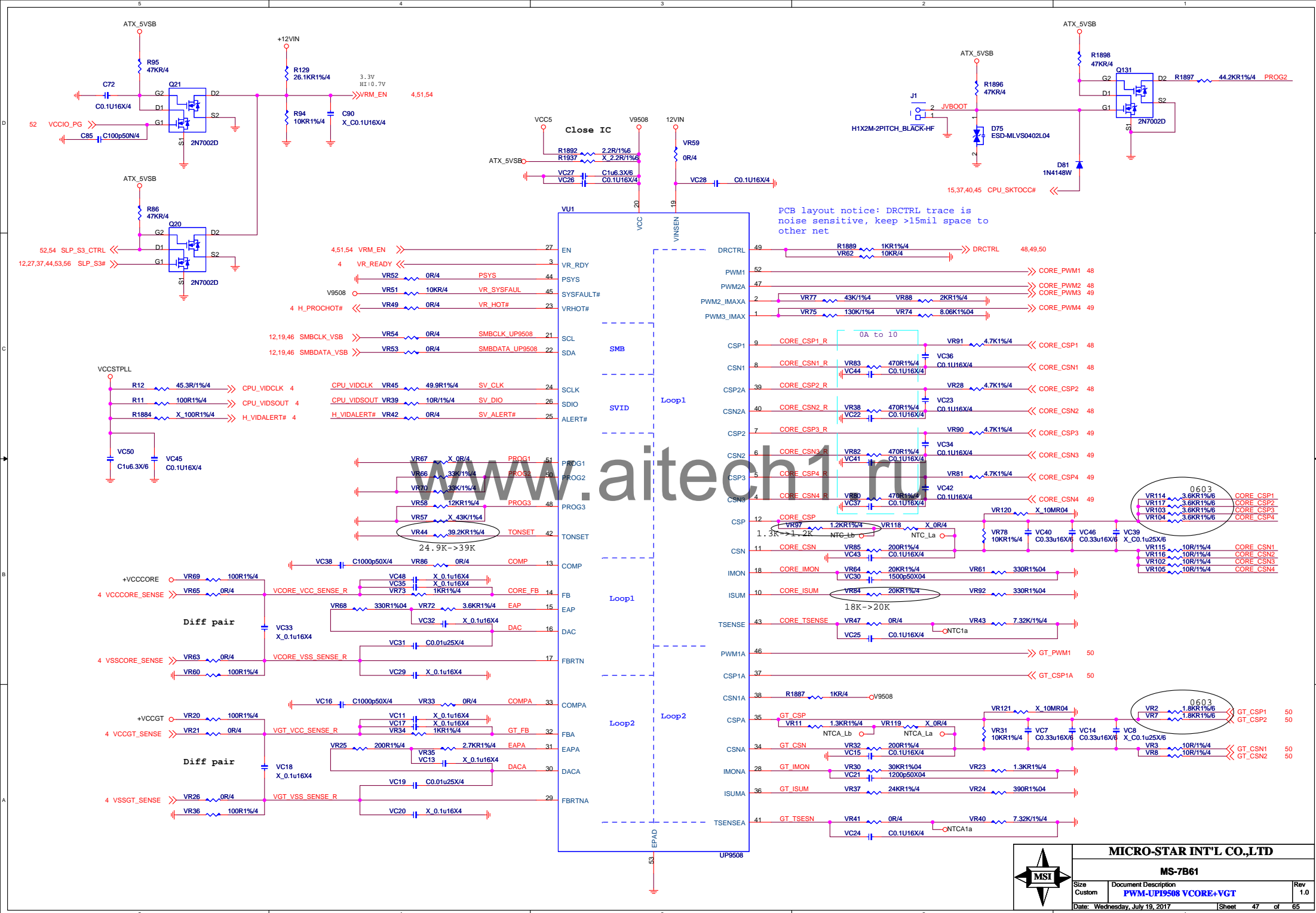
Date: Wednesday, July 19, 2017 | Sheet 45 of 65

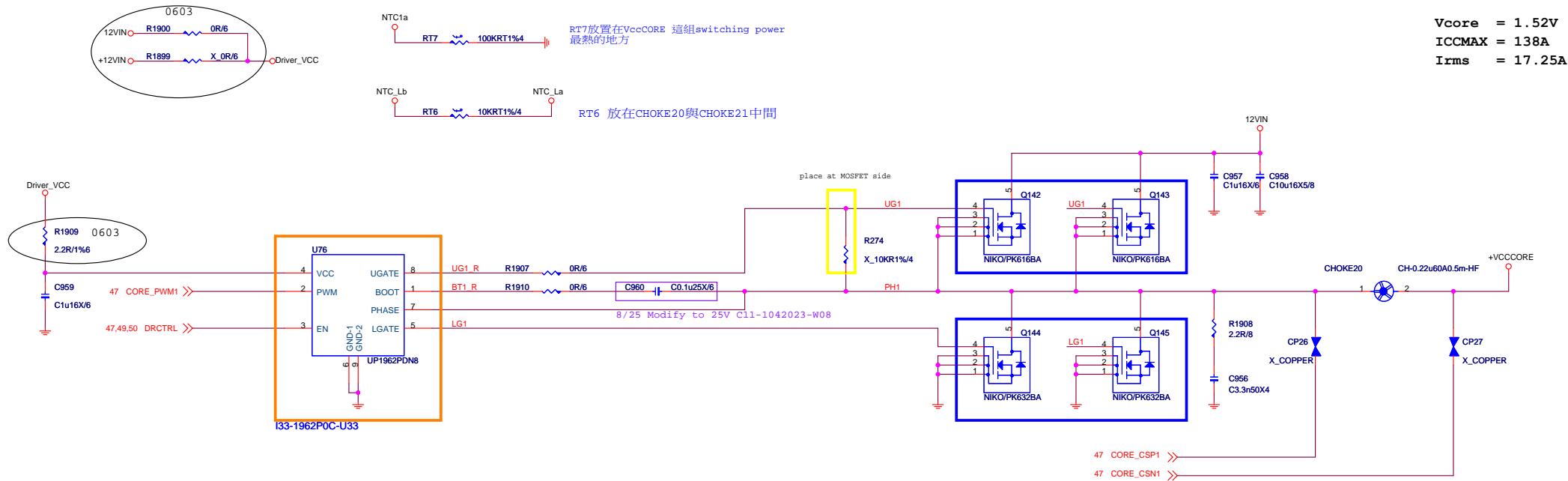
0x26:RH=18K,RL=13K



I34-3933U09-N62

	MICRO-STAR INT'L CO.,LTD		
	MS-7B61		
	Size Custom	Document Description OV-NCT3933	Rev 1.0
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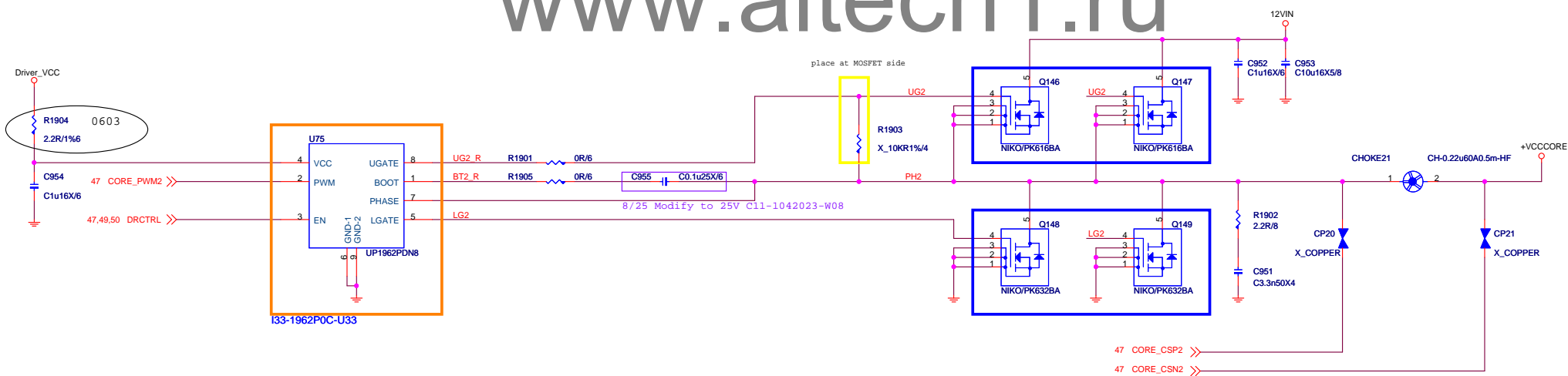


Vcore = 1.52V

ICCMAX = 138A

Irms = 17.25A

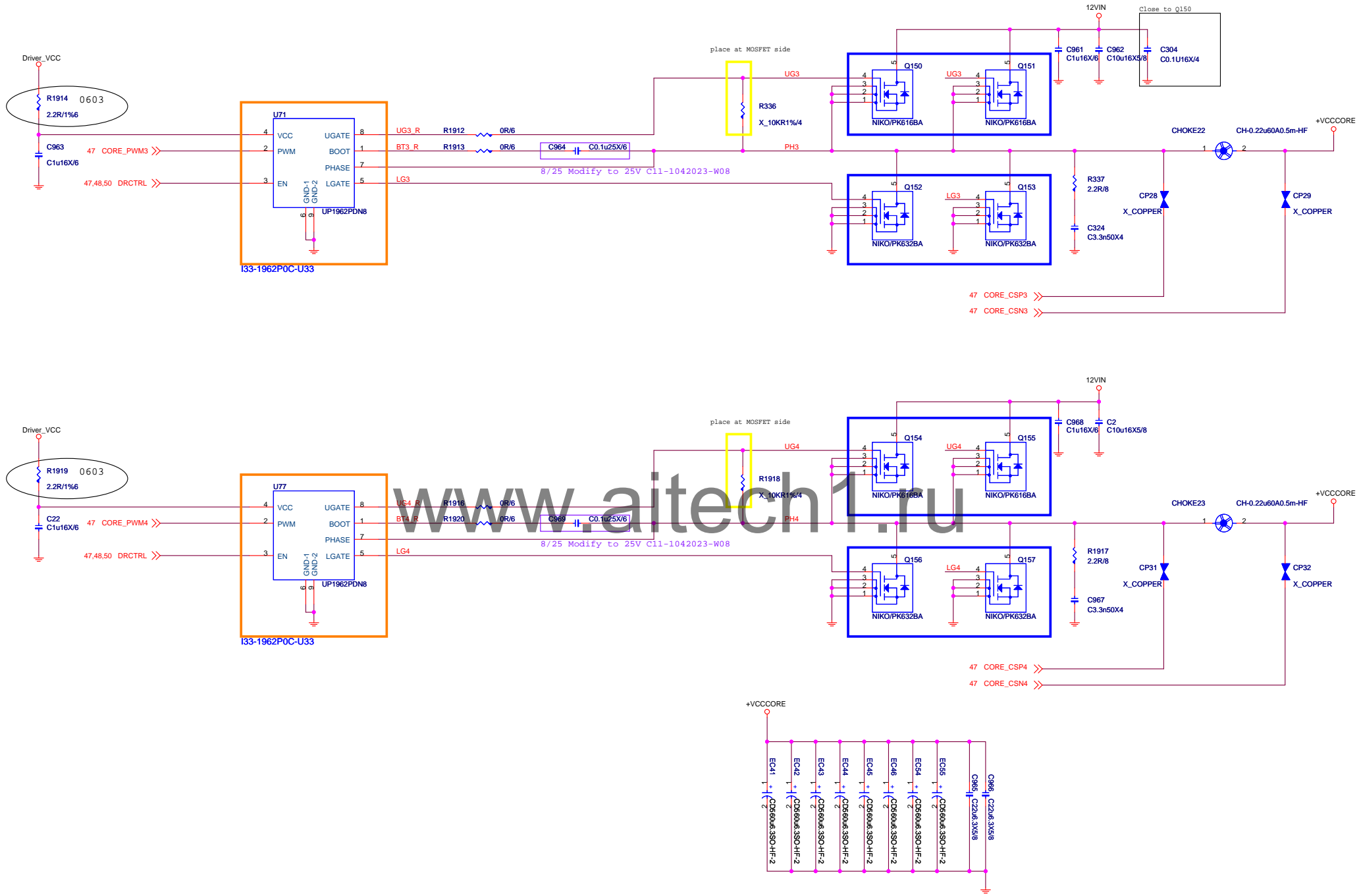
www.aitech1.ru

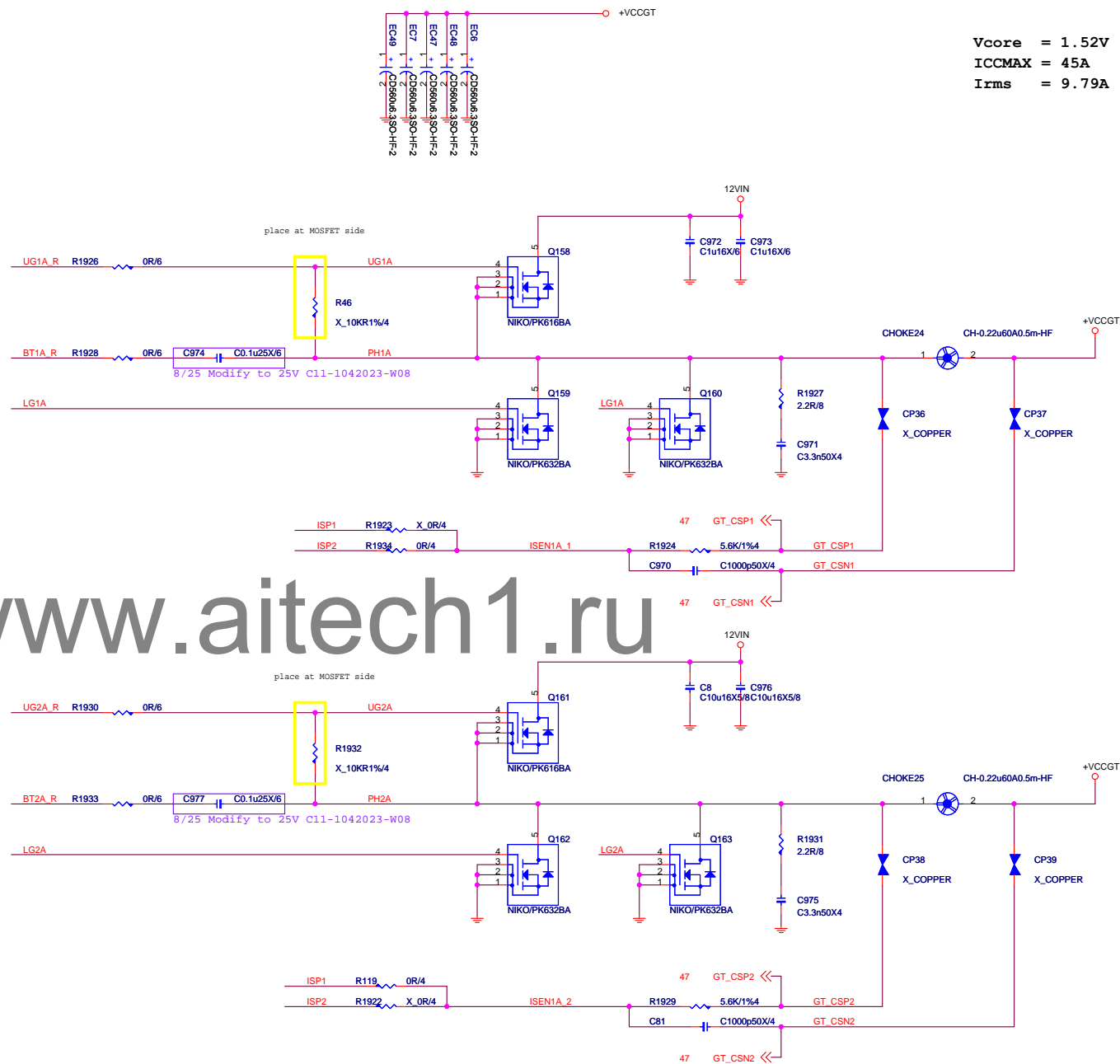
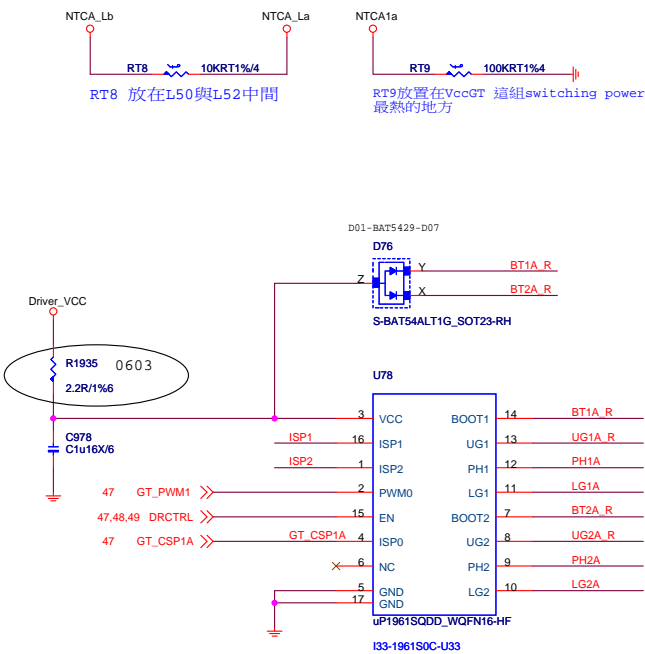


MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	VCORE - PHASE 1-2	1.0
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Vcore = 1.52V
ICCMAX = 45A
Irms = 9.79A

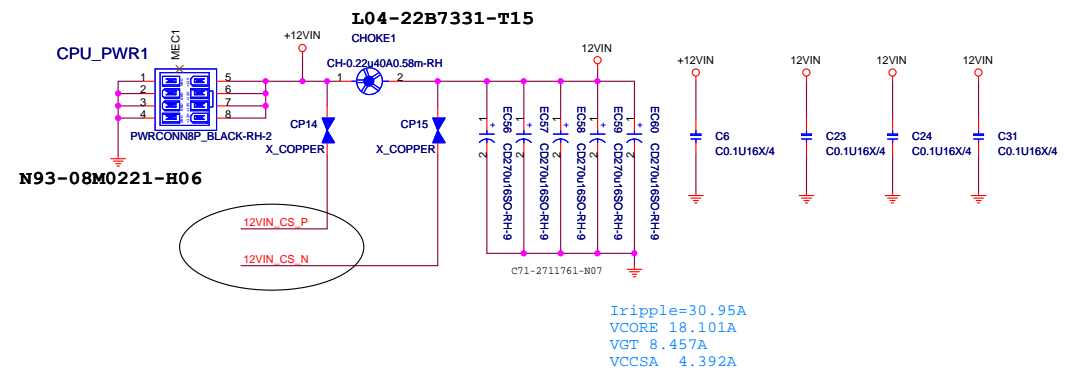
www.aitech1.ru



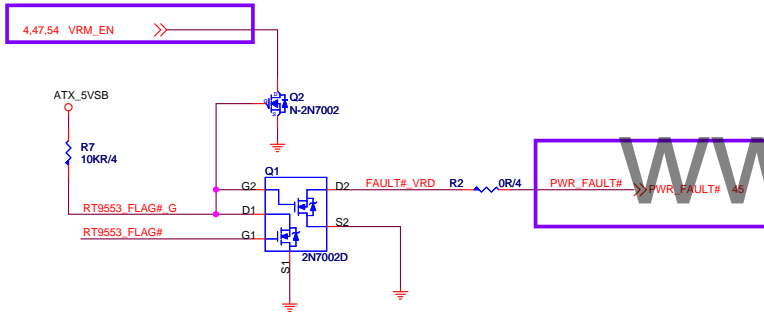
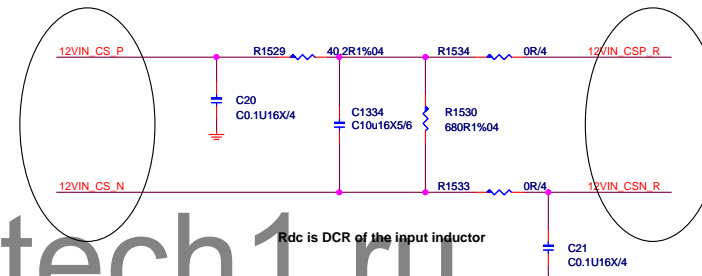
MICRO-STAR INT'L CO.,LTD

MS-7B61

Size	Document Description	Rev
Custom	VGTT MOS-PHASE 1-2	1.0
Date: Wednesday, July 19, 2017	Sheet 50 of 65	



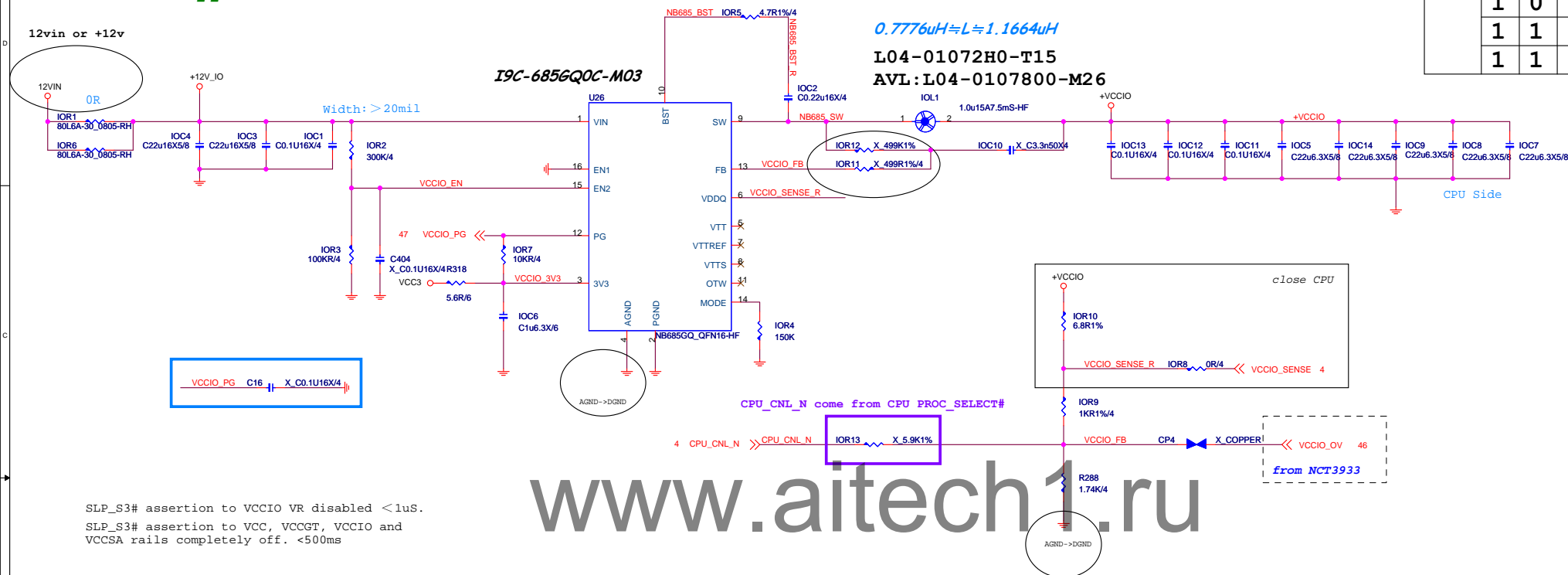
```
I3933_imon*[R17*R18/(R17+R18)]= Istep* RdcR*100
I3933_imon= 10uA/step
Istep=4.785A
```



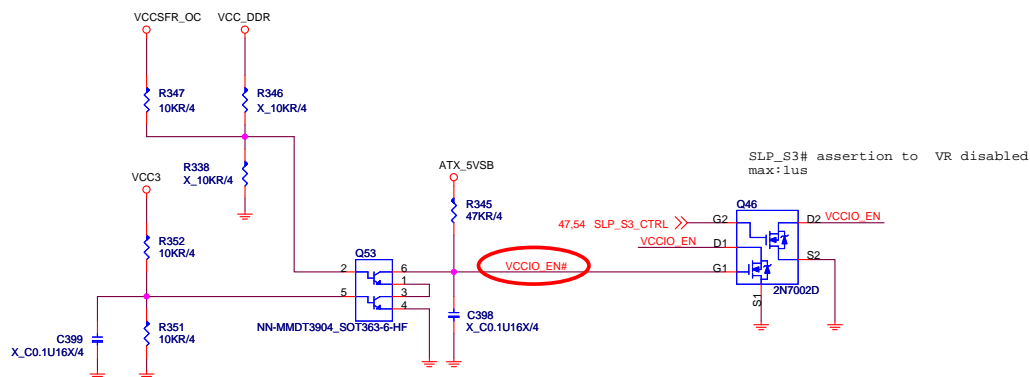
0.95V; 5.5A

support OV=>NB685

	LP#	C1	C0	VOUT (V)
VCCIO	0	X	X	0
	1	0	0	0.85
	1	0	1	0.875
	1	1	0	0.95
	1	1	1	0.975



```
SLP_S3# assertion to VCC, VCCGT, VCCIO and
VCCSA rails completely off. <500ms
```



MS-7B61

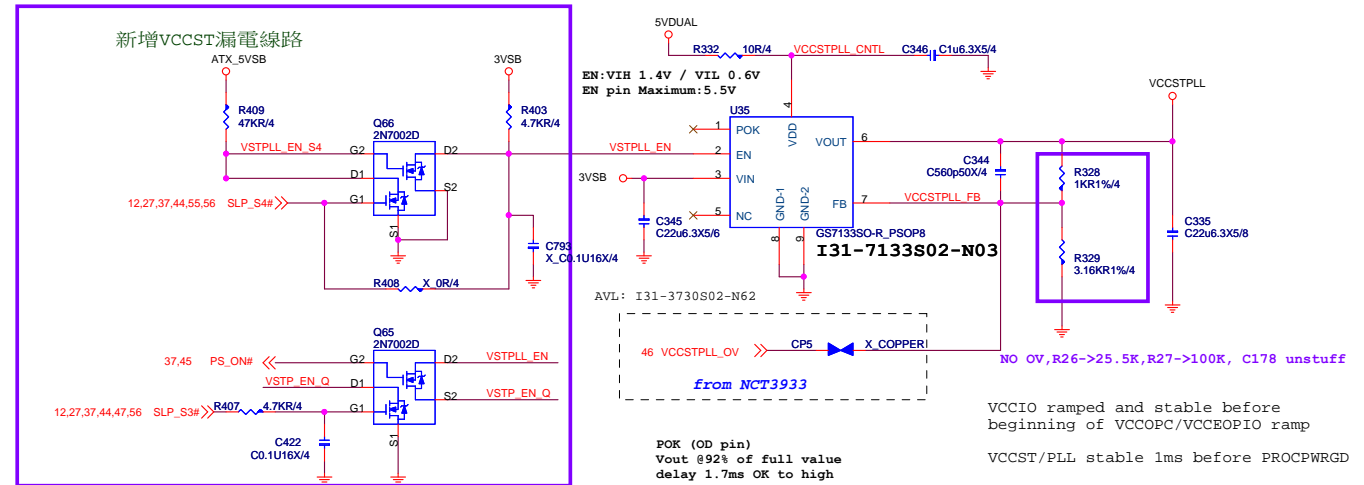
Size Custom	Document Description CPU PWR_VCCIO - NB681G	Rev 1.0
Date: Wednesday, July 19, 2017		Sheet 52 of 65

VCCSTPLL

1.0V; 250mA

For Cost down VCCST&VCCPLL merge

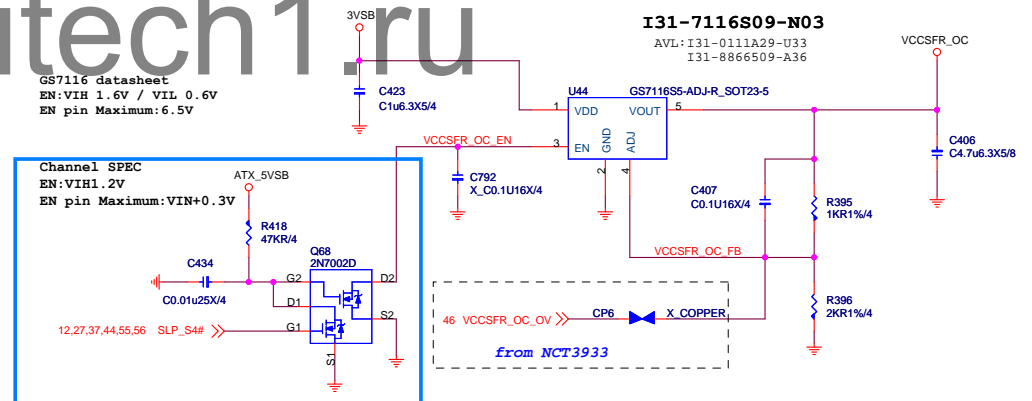
for Gaming3/5, Classic, ECO
and H110



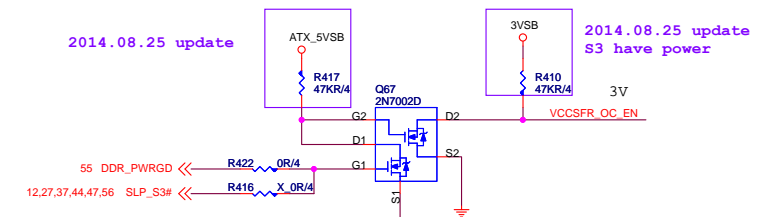
VCCPLL OC

1.2V; 110mA

2014.08.21 update



2014.08.25 update



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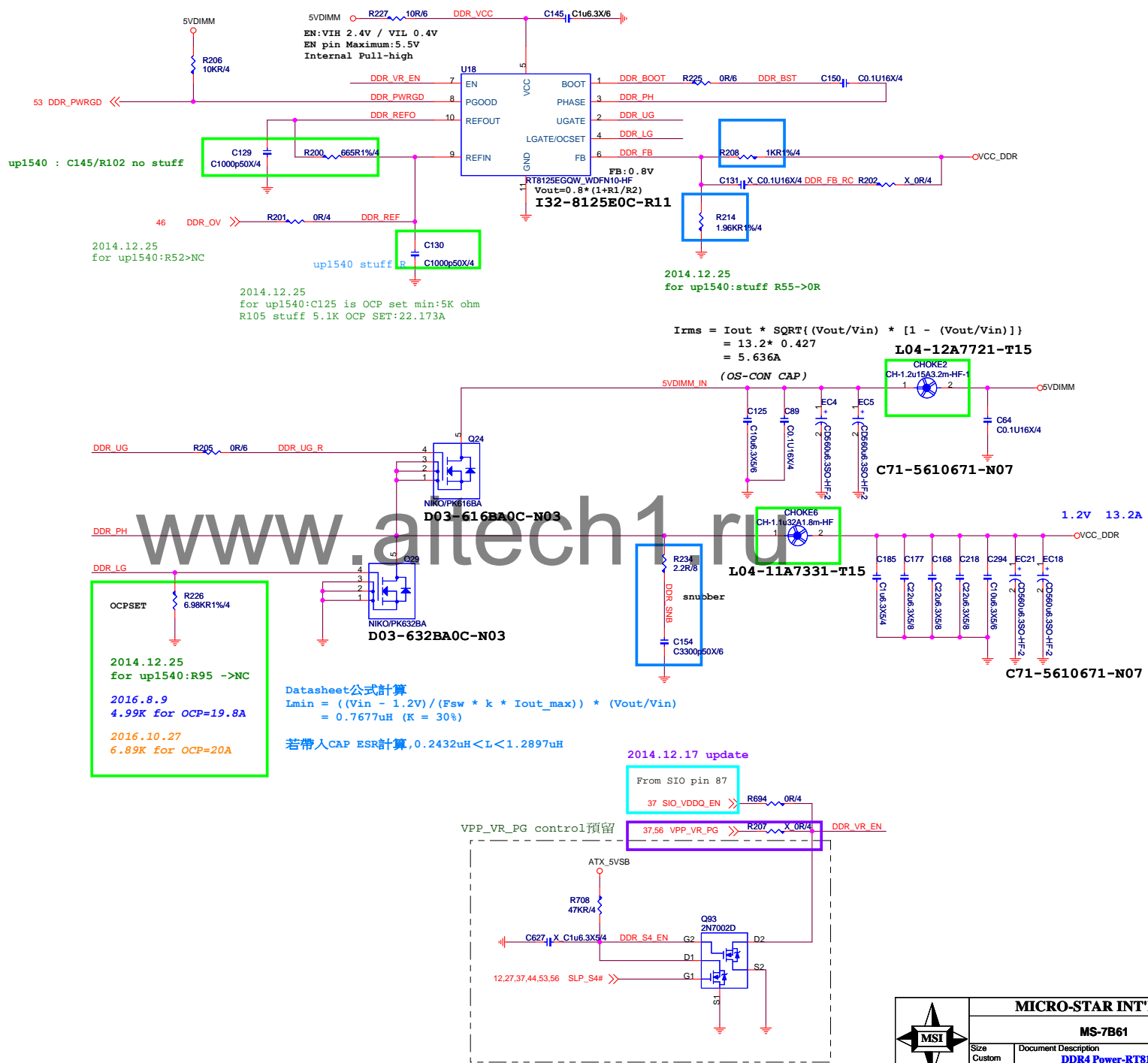
Size	Document Description	Rev
Custom	CPU PWR ST/PLL	1.0
Date: Wednesday, July 19, 2017	Sheet 53 of 65	

DDR4_1.2V 2.5A+9.5A+1.2A=13.2A
 2.5A FOR CPU
 9.5A FOR 4DIMM
 1.2A FOR DDR VTT

$OCP = 13.2A \times 1.5 = 19.8A$
 $Rocs(R3) = OCP \times R_{dson}[(Low\ side)/2]/10\mu A$
 $= 19.8A \times (4.6/2)m\Omega / 10\mu A$
 $= 4.95K\Omega < 5K\Omega$

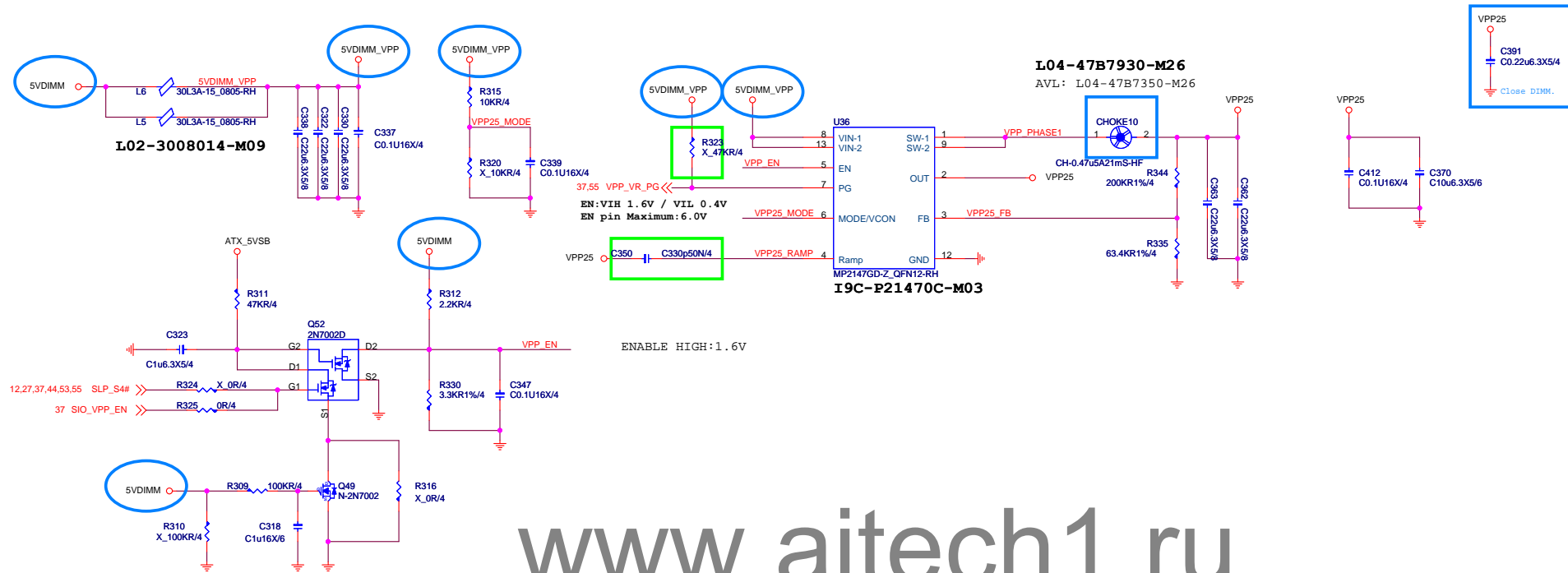
$Rocpset = 4.3K$
 $OCP = Rocset \times R_{dson}(Low\ side) / 10\mu A$
 $= 4.75K \times 4.6m\Omega / 10\mu A$
 $= 21.85A$

Rdson (low) 4.5V	
D03-4C05N03-005	: 5 mohm
D03-632BA0C-N03	: 4.6mohm
D03-3056M00-U47	: 6.2mohm



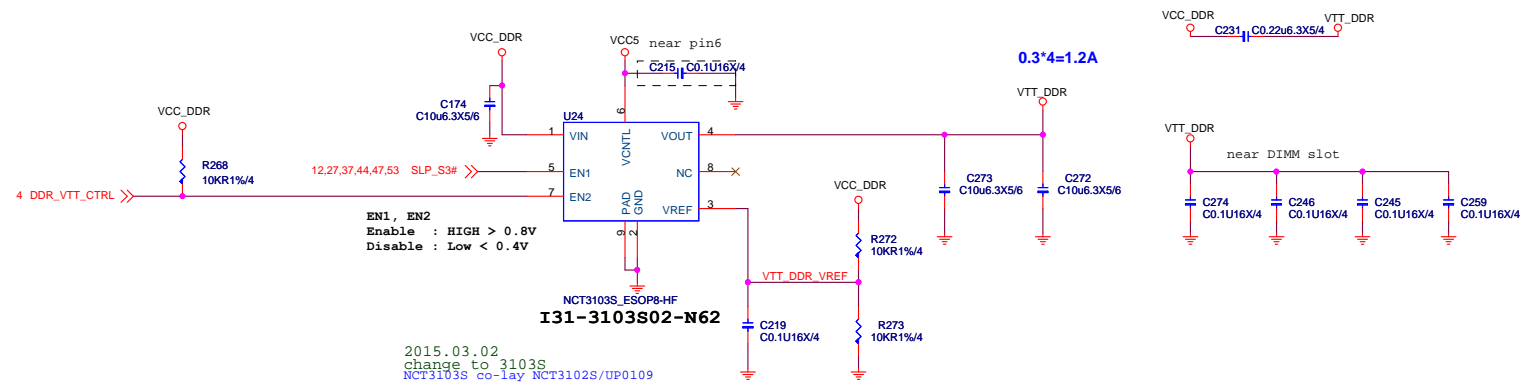
4DIMM :2.24A FOR DDR VPP2.5V

VPP25 Power
2.5V; 2.24A



To make sure VPP EN after 5VDIMM stable

DDR VTT Power



MICRO-STAR INT'L CO.,LTD

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Size Custom	Document Description DDR4 Power-VPP25	Rev 1.0
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PCH 1VSB

1.0V; 11A

OCP = 16.69A

OCP = $10\mu A \times 7.68K / 4.6 \text{ mohm}$
= 16.69 A

Rocs: 7.87K, OCP:

D03-4C05N03-O05 : 15.74A

D03-632BA0C-N03 : 17.1A

use UBIQ MOS need Check

Rdson(low side mosfet) 4.5V

D03-3116M00-U47 : 3.6 mohm

D03-632BA0C-N03 : 4.6mohm

D03-3056M00-U47 : 6.2mohm

EN: VIH 2.4V / VIL 0.4V
EN pin Maximum: 5.5V
Internal Pull-high

2014.08.21 update

PCH REFOUT

2014.08.25: Change 1u/0603

2014.12.25

For up1540: C236&R204 -> NC

2014.12.25

For up1540: C193 is OCP set min: 5Kohm

R185 stuff 7.87K OCP SET: 15.74A

2016.8.9

4.22K for OCP=16.69A

2016.10.27

5.62K for OCP=17.8A

2016.8.9

4.22K for OCP=16.69A

2016.10.27

5.62K for OCP=17.8A

2016.8.9

4.22K for OCP=16.69A

2016.10.27

5.62K for OCP=17.8A

2016.8.9

4.22K for OCP=16.69A

2016.10.27

5.62K for OCP=17.8A

2016.8.9

4.22K for OCP=16.69A

2016.10.27

5.62K for OCP=17.8A

2016.8.9

4.22K for OCP=16.69A

2016.10.27

5.62K for OCP=17.8A

2016.8.9

4.22K for OCP=16.69A

2016.10.27

5.62K for OCP=17.8A

2016.8.9

4.22K for OCP=16.69A

2016.10.27

5.62K for OCP=17.8A

2016.8.9

4.22K for OCP=16.69A

2016.10.27

5.62K for OCP=17.8A

2016.8.9

4.22K for OCP=16.69A

2016.10.27

5.62K for OCP=17.8A

2016.8.9

4.22K for OCP=16.69A

2016.10.27

5.62K for OCP=17.8A

2016.8.9

4.22K for OCP=16.69A

2016.10.27

5.62K for OCP=17.8A

2016.8.9

4.22K for OCP=16.69A

2016.10.27

5.62K for OCP=17.8A

2016.8.9

4.22K for OCP=16.69A

2016.10.27

5.62K for OCP=17.8A

$$V_{out} = V_{ref} * (1 + R_{821}/R_{822})$$

$$= 0.8 * (1 + 1K/3.92K)$$

$$= 0.8 * 1.2551$$

$$= 1.004V$$

L04-47B7730-T15 for OC, Gaming 10, 9, 7, 5
L04-12A7321-L65 for Gaming 3, SLI, ECO
L04-12A7721-T15 for cost down

L02-3008014-M09

L10 30L3A-15 0805-RH
L9 30L3A-15 0805-RH

too Big
C651 X_C0.1U16X/4

MAX: 10.664A

C71-5610671-N07

D03-616BA0C-N03

D03-632BA0C-N03

CH-1.0U14A5.5mS-HF

2016.08.15

change used

L04-01073F0-M26

AVL: L04-0107800-M26

C71-5610671-N07

$$I_{min} = ((V_{in} - V_{out}) / (F_{sw} * k * I_{out_max})) * (V_{out}/V_{in})$$

$$= 0.8335\mu H \text{ (K = 30\%)}$$

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MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	PCH Core Power-RT8125E	1.0
Date: Wednesday, July 19, 2017	Sheet 57 of 65	

PCB



7B61_1.0

PD0-07B6110-G37

PD0-07B6110-E48

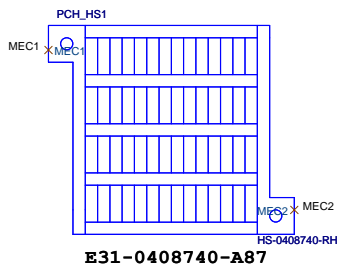
CPU Socket metal sheet

CPU_H1



CPU_H1

E21-7869020-F02



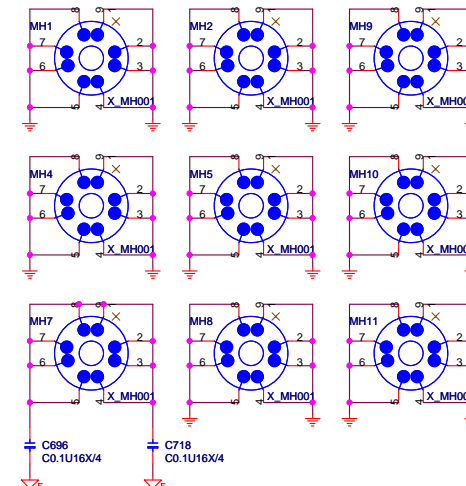
MEC1 MOS-W_HS1

MEC2

HS-0P505260-HF
<Value_MC>

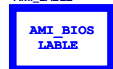
E31-0504590-A87

Mounting Holes



BIOS Label

AMI_LABEL



BIOS_LABEL

G51-M1SPXXA-A09

CFOS Label

TABLE1



CFOS

Y02-MU00170-CFO

XSPLIT Label

TABLE2



X_SPLIT

Y02-MA00401-XSP

SSE Label

TABLE3



SSE

Y02-MA00101-SSE

MKT Label

TABLE4

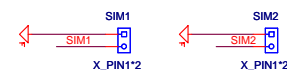


MKT

G51-M1SPK88-Q13

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Simulation



Test point



Optical Fiducial Marks-120

